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Sigma-delta digital-to-alalog converter frequency smoothing using a filtering switched-capacitor-3-level converter

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Sigma-Delta Digital-to-Analog Converter Frequency Smoothing Using a Filtering Switched-Capacitor-3-level Converter

by

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TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

ABSTRACT

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This thesis introduces a new low pass filtering technique for use with a Sigma-Delta type Digital to Analog Converter (DAC) for digital audio applications. This technique combines a Finite Impulse Response (FIR) lowpass filter with a one-bit Switched-Capacitor DAC. Introducing filtering earlier in the conversion process eases the requirements for the analog post-filtering since the FIR filter has already provided a sharp cutoff for the passband and a linear phase response. Presented in this thesis is a short synopsis of digital audio, FIR filtering and present audio digital to analog conversion techniques. Followed by the development of the proposed FIR DAC architecture. Finally recomendations for further work is presented.

1.0 Introduction and Background Theory

For Digital Audio products, cost and performance are two major factors affecting success and popularity. Improving a product's performance typically increases its complexity and cost, which can reduce its potential market. Sigma-Delta based Digital-to-Analog Converters (DAC) are unique in that they exhibit improved performance with reduced analog circuitry complexity. They achieve this performance by using an internal architecture that operates many times faster than the original sampling rate. Increasing the internal operating speed has its drawbacks though, one of which is the generation of large amounts of out-of-band noise. A disadvantage of present Sigma-Delta DAC's is that an analog low pass filter with a sharp and well controlled cutoff is needed at the passband edge to remove this out-of-band noise energy. If the high frequency quantization noise energy could be further reduced before the signal is converted into the analog domain, the analog post filtering requirements would be much easier to meet, thus making Sigma-Delta DACs even more economical to manufacture.

For this thesis, since Sigma-Delta based DACs have many desirable properties, a method for reducing the undesirable out-of-band energy is presented. In this method, the usual one-bit switched-capacitor DAC is also used as a FIR lowpass filter. By introducing filtering in the DAC stage, the analog post-filtering requirements can be relaxed.

The following sections present a discussion of Digital Audio, Sigma-Delta modulation and Finite Impulse Response (FIR) filters.

1.1 What is Digital Audio

Digital audio is a means of representing audio frequency signals (0 - 20kHz) by a sequence of digital words typically 16-bits long [1]. The digital words are obtained by sampling and quantizing the original analog signal at a uniform rate slightly above the Nyquist frequency, typically 44.1 kilo-Samples per second (kS/s). Representing audio in this form has many advantages such as:

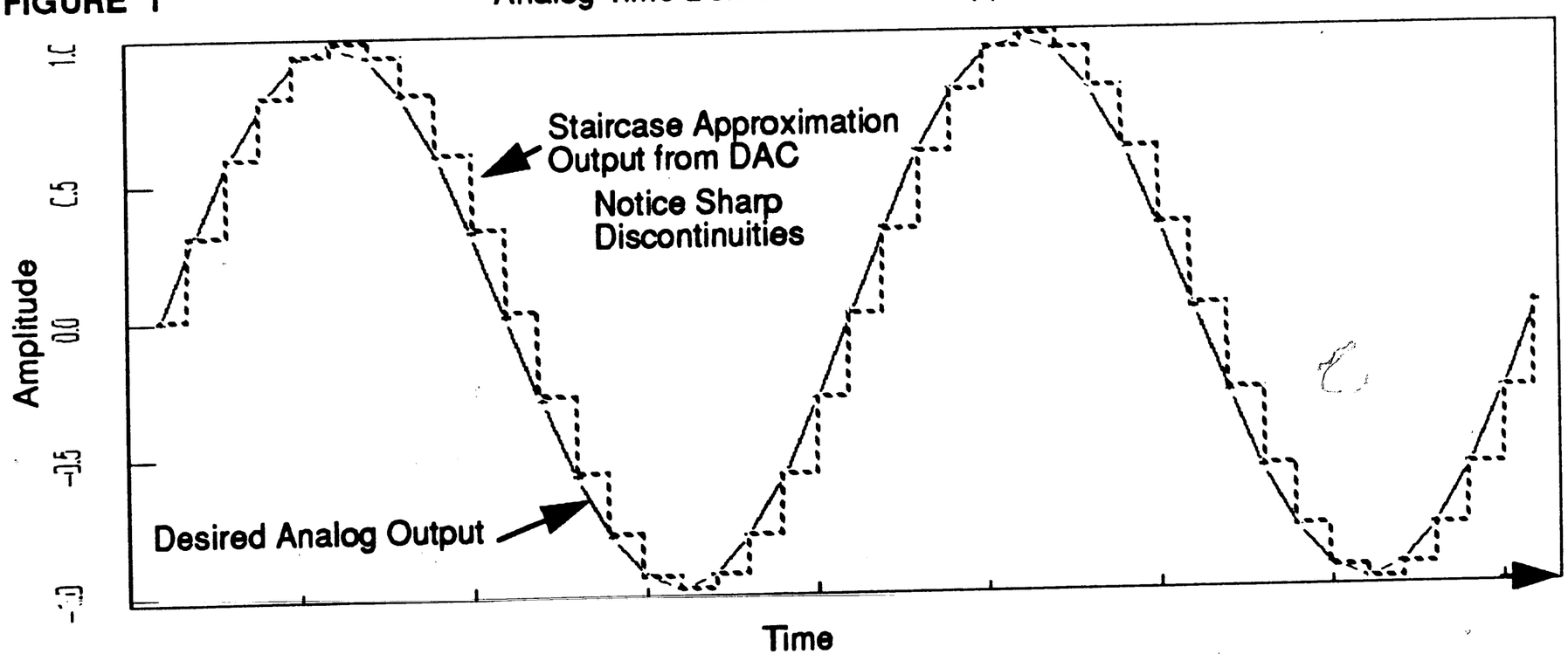
- No signal degradation or added noise as the audio is repeatedly copied, played or processed.

- The Signal to Noise or Distortion ratio of the recording media is fixed by the 16-bit quantization.
- The digital data is encoded in a manner such that damage to the recording media and resulting loss of short segments of data does not produce objectionable outputs.

For a digital audio quality signal, it is desirable that over the entire baseband the amplitude response remain constant and phase response be linear. Outside the baseband, it would be desirable for no energy to be present. Conventionally when a digital audio recording is played, the digital words are applied to a Nyquist rate DAC, which converts the digital data into a staircase shaped analog approximation as shown in FIGURE 1. In using the term Nyquist rate DAC, it is implied that data is applied to a 16-bit converter operating at the original sampling rate.

The sharp discontinuities of the analog staircase approximation shown in FIGURE 1 cause a large amount of energy to be present at frequencies above one-half the Nyquist rate. This signal not only contains the original baseband energy, but also contains energy located about the sampling rate frequency and its multiples (images) as shown in FIGURE 2. Also shown in FIGURE 2 is the desired frequency response for a reconstruction or lowpass filter which attenuates these image frequencies. After passing through the reconstruction filter, the signal spectrum appears as shown in FIGURE 3.

FIGURE 1 Analog Time Domain Staircase Approximation of a Sinusoidal Signal.



If the energy at frequencies above the baseband is not attenuated, the analog output buffers and amplifiers are required to slew faster than necessary, which can cause distortion of the baseband signal.

It is also possible that intermodulation of the image frequencies could result in added baseband noise or spurious signals within the baseband. Note that the reconstruction filter must attenuate the first image by 60dB or more and is only given 4.1 kHz over which to transition from zero attenuation to greater than 60dB of attenuation. This requires a filter with many poles. To achieve acceptable performance would require using tight tolerance components, possible hand tuning and a phase equalizer. Considering the required cutoff and transition requirements needed for the reconstruction filter, obtaining a constant passband amplitude and linear phase response will be difficult.

FIGURE 2 Frequency Spectrum of a D/A Converted Digital Audio Signal Without a Reconstruction Filter.

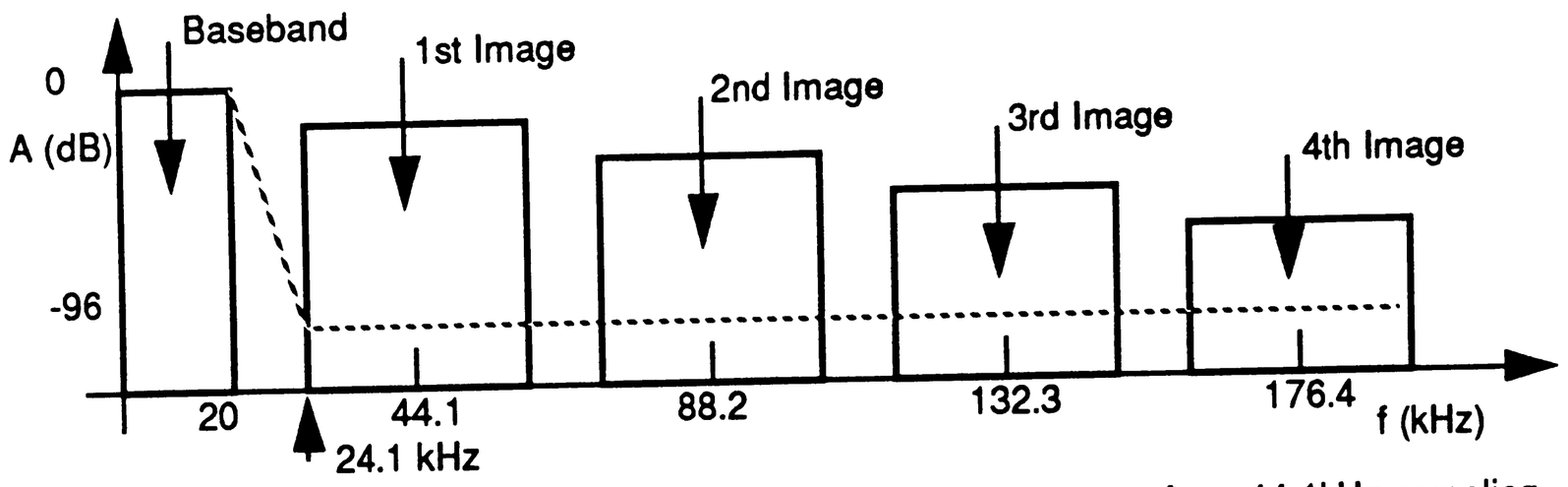
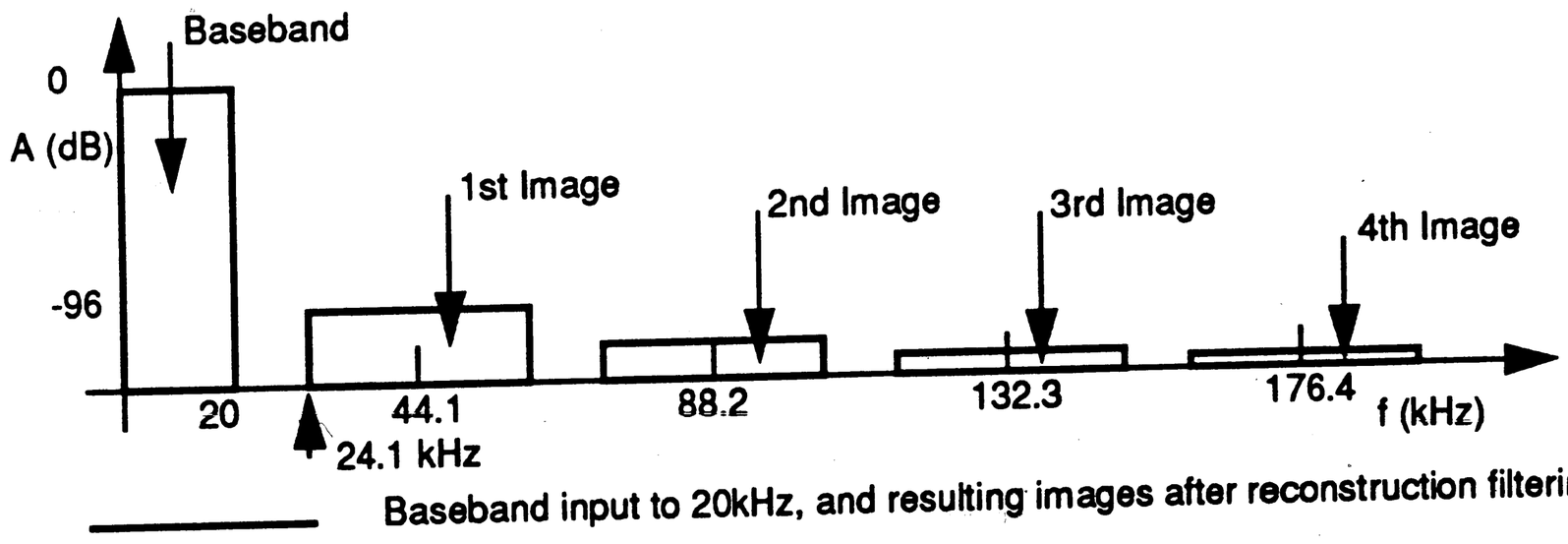


FIGURE 3 Desired Frequency Spectrum of a D/A Converted Digital Audio Signal After Reconstruction Filtering.



The 16-bit DAC is a large part of the manufacturing cost for a classical Nyquist rate digital audio system. Multi-bit DACs depend upon device matching or calibration for low harmonic distortion (linearity), both of which are costly to implement.

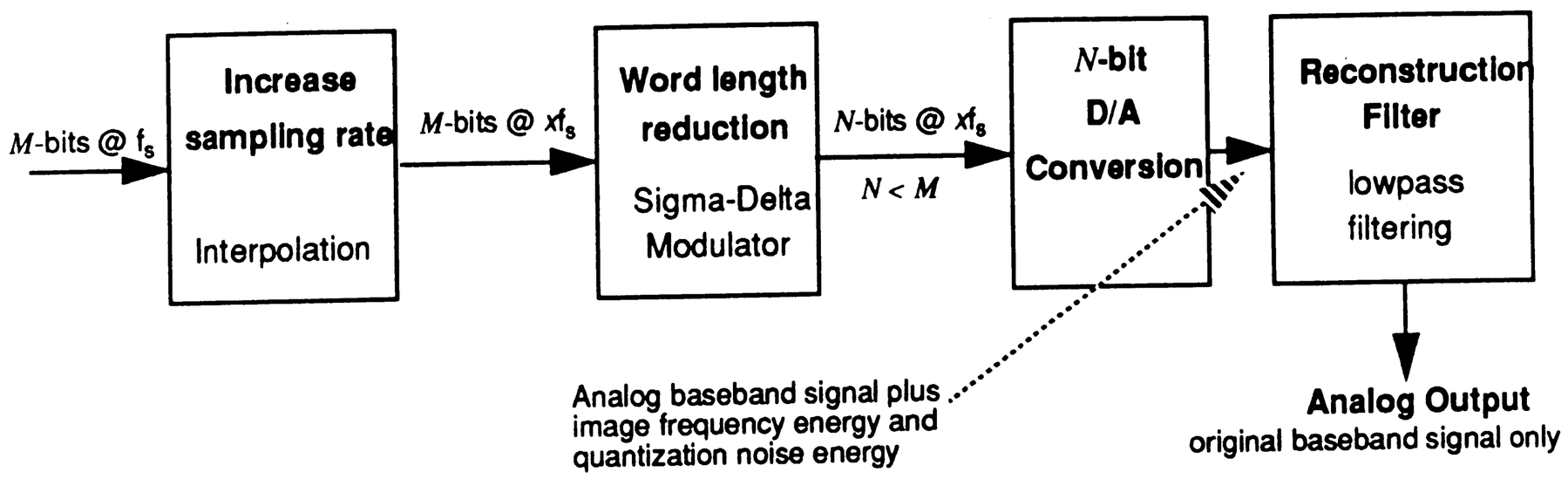
1.2 One-bit Digital to Analog Converters

Since multi-bit DACs are not inherently linear, how can a DAC with inherent linearity be realized. For inherent linearity only two output levels can be defined by the DAC. To see how perfect linearity results it is necessary to plot the output transfer function (analog output level vs. code input) for the one-bit DAC. Perfect linearity results by having a straight line connect all the points of the transfer curve, which is not difficult since there are only two points. This is not the case for a multi-bit converter, since to have all the points of the transfer curve fall upon one straight line is difficult. For a one-bit converter, only the + and - full scale reference levels need to be defined. Since there are only two possible output levels, intermediate output levels (at a reduced conversion rate) can be generated by switching the output between these reference these levels in an appropriate sequence. The switching needs to be done at a high rate such that the average value produced over a longer time will be the desired intermediate output level. For each intermediate output level desired, a different sequence of switching between the reference levels is needed.

1.3 What is and Why Use Sigma-Delta Modulation

For a one-bit converter to be useful in a digital audio system requires that the incoming Nyquist rate multi-bit data be reduced to one-bit precision yet still produce an output signal quality equivalent to the original 16-bit data. Therefore the one-bit input rate to the DAC must be many times the original quantization rate to allow for averaging to produce the intermediate levels. An oversampled Sigma-Delta DAC is a circuit architecture which accomplishes the translation of the original 16-bit signal into one which can drive the one-bit DAC and produce an output signal equivalent to the original input.[2-5]. FIGURE 4 presents this architecture in a generalized fashion showing that it is also useful for data length reductions to other levels besides one-bit.

FIGURE 4 Theoretical Block Diagram of a Oversampled Sigma-Delta DAC



In simple terms a Sigma-Delta modulator converts a M-bit wide data stream into a N-bit wide data stream where $N < M$ but at the same word rate. Since the Sigma-Delta modulator does not change the word rate, the input first passes through an interpolation stage, which increases the word rate by generating additional samples between known sample points. An interesting point is that the word length can be reduced to any desired value between (M -1)-bits and 1-bit. Although the word length is reduced, the DAC must still have a linearity equal to the original M-bit level unless other special system architectures are used. For example, if the word length is reduced from 16-bits to 4-bits, the 4-bit DAC must have its intermediate output levels accurate to a 16-bit level. For this reason it is advantageous to reduce the word length to 1-bit since a 1-bit DAC is inherently linear. A typical Sigma-Delta based DAC used for Digital-Audio applications would accept 16-bit data @ 44.1kHz rate, interpolate by a factor of 256, increasing the data rate to 16-bits @ 11.28MHz and then reduce the word length to 1-bit @ 11.28MHz with a Sigma-Delta modulator whose output in turn controls a one-bit DAC and following filter.

1.3.1 Sigma-Delta Modulation in the Frequency Domain

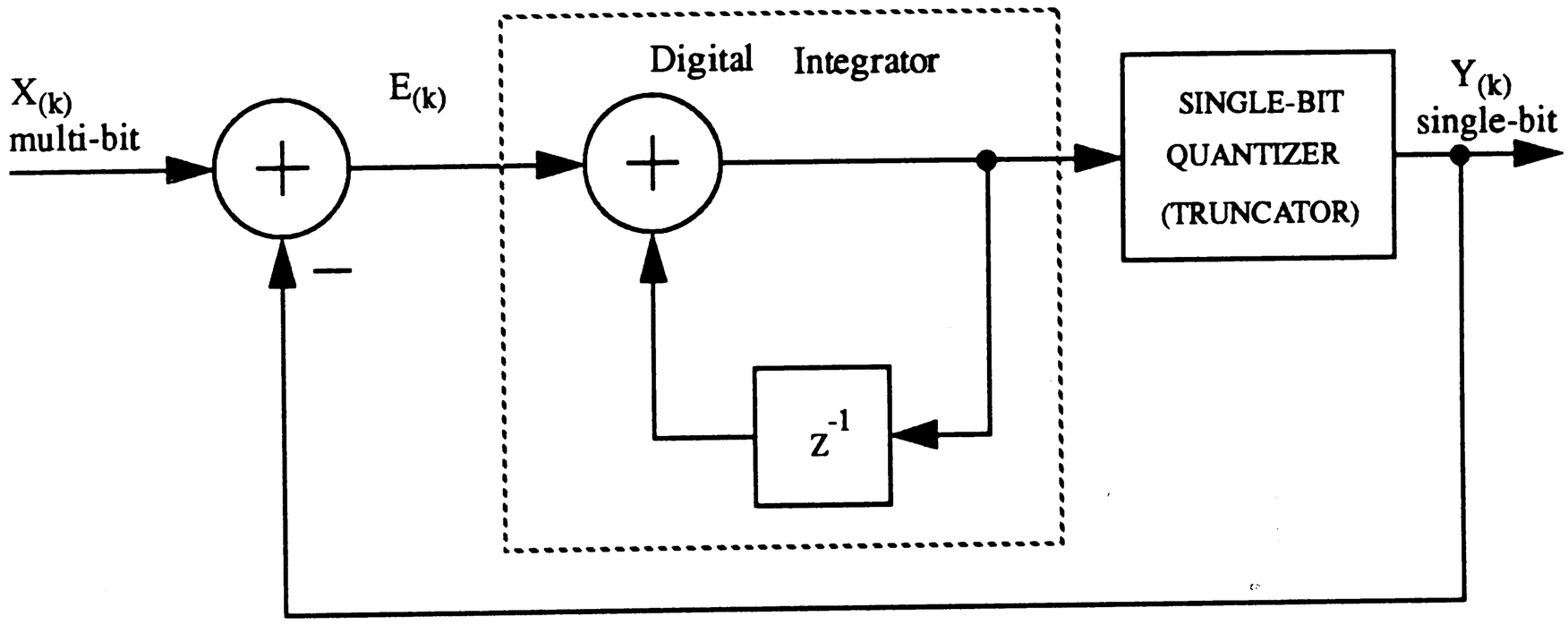
To investigate what Sigma-Delta modulation does to the frequency spectrum of applied signals, a computer simulation of a first-order modulator will serve as an example. An architecture which can be used for this modulator is shown in FIGURE 5. This circuit converts multi-bit input data into one-bit

data at the output. The input data to the modulator $X_{(k)}$ is first differenced with the previous one-bit quantized output $Y_{(k)}$ to form an error signal $E_{(k)}$ represented by:

$$E_{(k)} = X_{(k)} - Y_{(k)} \qquad \text{(EQ 1)}$$

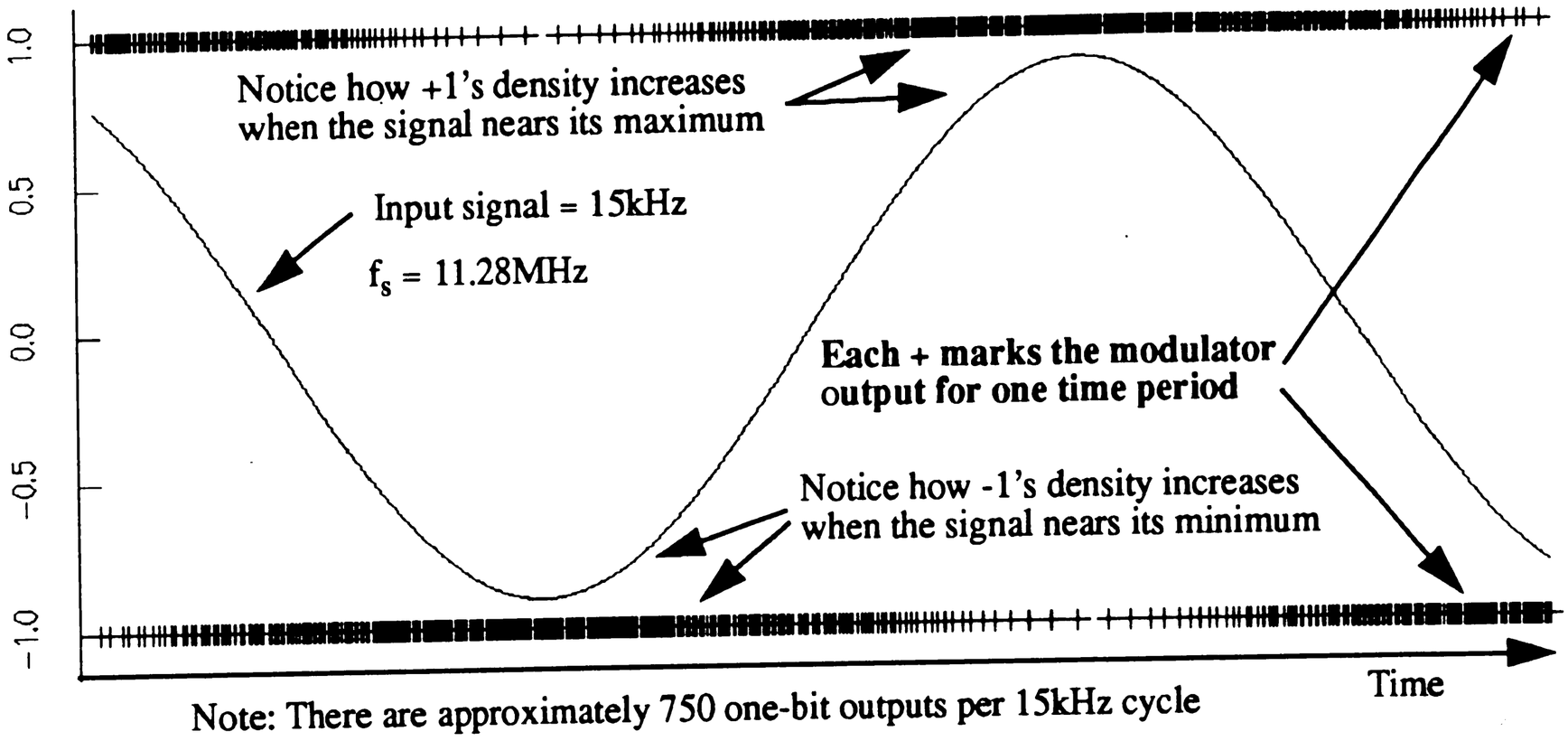
This error signal is then integrated by the digital integrator and quantized into one of two possible outputs. The quantizer output is also used as digital output of the modulator. Since the modulator operates with binary numbers, the quantizer could be a truncator such that the MSB determines its output. The modulator tries to keep the average value of the error near the quantizer switch point.

FIGURE 5 Functional Block Diagram of a First-Order Sigma-Delta Modulator



Next by applying a signal to the modulator shown in FIGURE 5 and observing its output in the time and frequency domains, the quantization noise shaping and large amount of high frequency energy become observable. The input signal to the modulator is a -0.9dB 15kHz sine wave quantized at 11.28MHZ and the modualtor is being clocked at 11.28MHZ (256 x 44.1kHz).

FIGURE 6 Time Domain Output of a First-Order Sigma-Delta Modulator

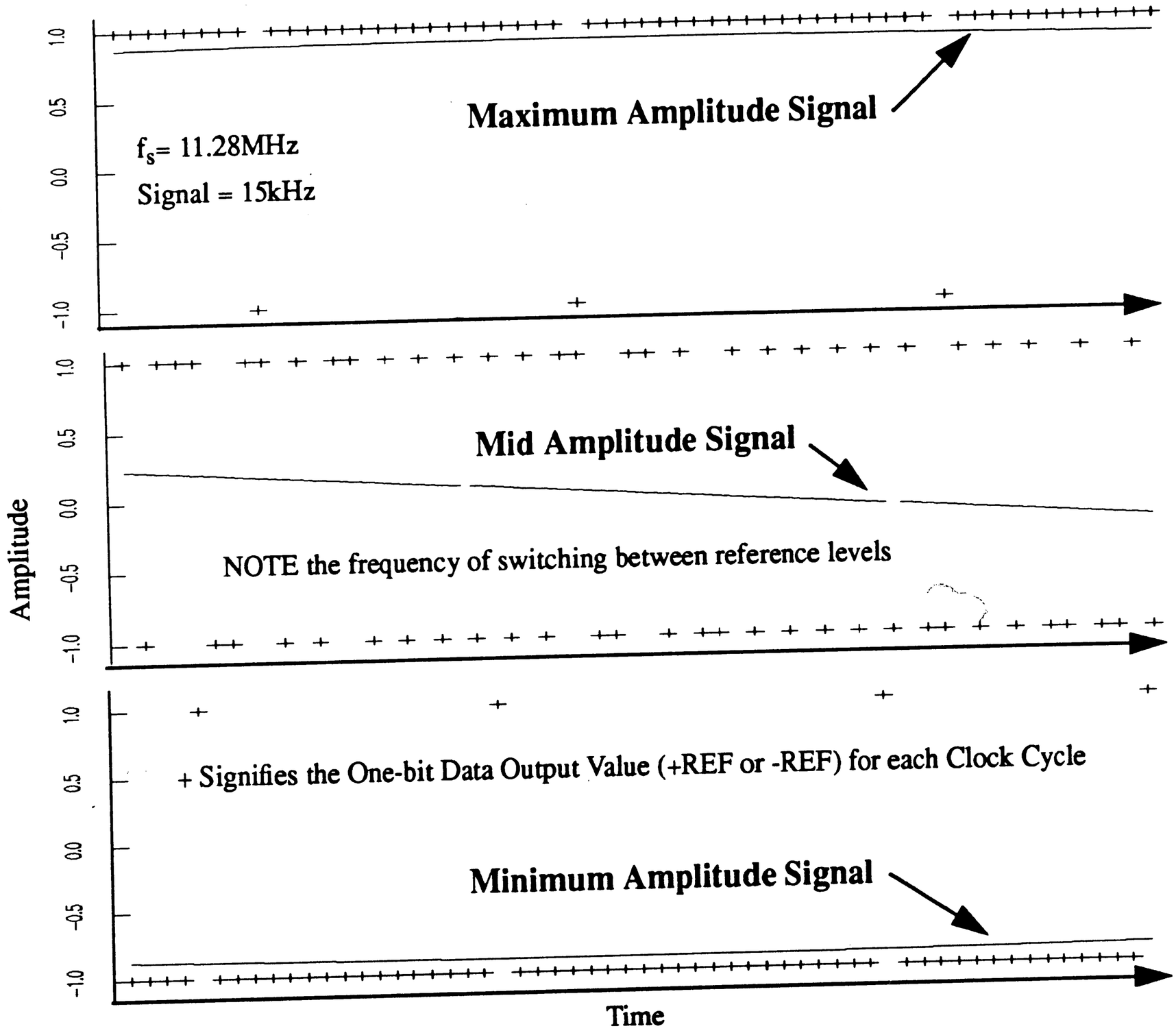


Note: There are approximately 750 one-bit outputs per 15kHz cycle

FIGURE 6 shows the quantized analog input and the one-bit output both plotted on the same scale. It is important to notice that the output is constantly changing between the two levels. Also notice that as the input level nears either end of the conversion range, the frequency of occurrence of the opposite output level diminishes. If the one-bit output of the modulator were applied to a lowpass filter with a cutoff at 20kHz, the original input signal would be observed.

FIGURE 7 shows with an expanded time scale the input and output of the modualtor for three levels of signal input. The top plot shown the output when the input signal in near its maximum. Note the increased number of upper reference level outputs and correspondingly reduced number of lower reference level outputs. The middle plot shows a mid-level input and near equal number of both output levels. The lower plot shows the output when the input is near its minimum. Note the increased number of lower reference level outputs and correspondingly reduced number of upper reference level outputs.

FIGURE 7 Sigma-Delta Modulator One-bit Output for Various Signal Amplitudes



In observing FIGURE 7, it is important to notice how often the one-bit output is changing between the two reference levels, when the input signal is near the mid-amplitude region. A good the rule of thumb for audio applications is to have the average RMS signal level approximately 20dB below the system clipping level. Following this rule, the normal RMS output level would normally be in this region of frequent output level switching. With this in mind, it is easy to see why there is a huge amount of high frequency energy generated by Sigma-Delta modulation. The less of this energy the output amplifiers must handle, the easier it will be to meet the desired performance.

FIGURE 8 Entire Frequency Spectrum of a First-Order Sigma-Delta Modulator

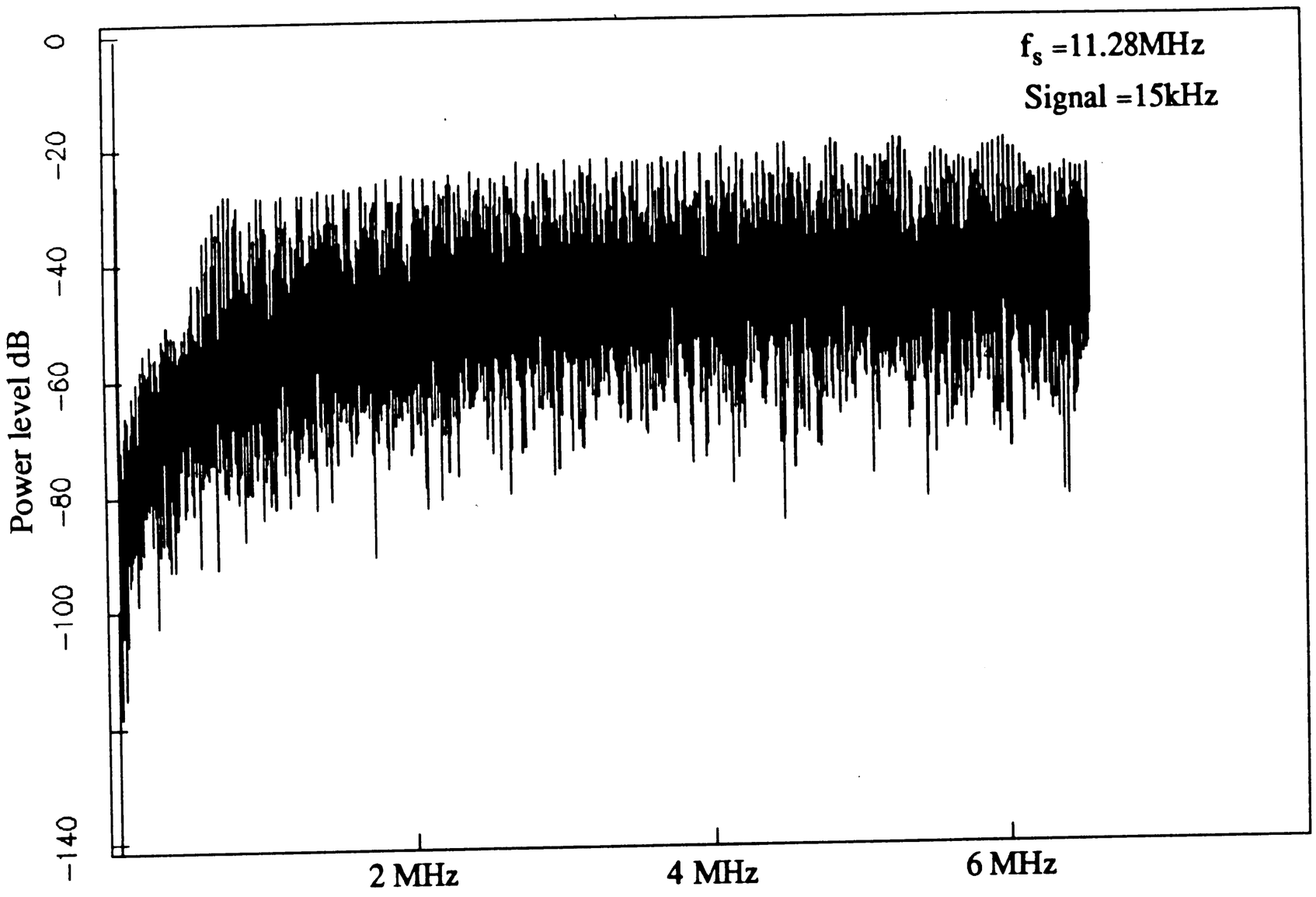


FIGURE 8 shows the entire frequency spectrum for the one-bit output of the first order modulator. Normally when a signal is quantized, the added quantization noise is considered to be white, with constant energy in each frequency interval, even the baseband. This would make a one-bit quantizer useless for 16-bit audio applications. Since the feedback around the Sigma-Delta modulator loop suppresses the quantization noise energy in the baseband, it becomes a one-bit quantizer that is capable of representing baseband signals with greater than one-bit precision. It is interesting to note how fast the noise power increases with increasing frequency. Since the baseband noise shape is controlled by the modulator architecture, much research has been done trying to determine the optimum modulator architecture [6], [7], [8].

FIGURE 9 Baseband Frequency Spectrum of a First and Second Order Sigma-Delta Modulator

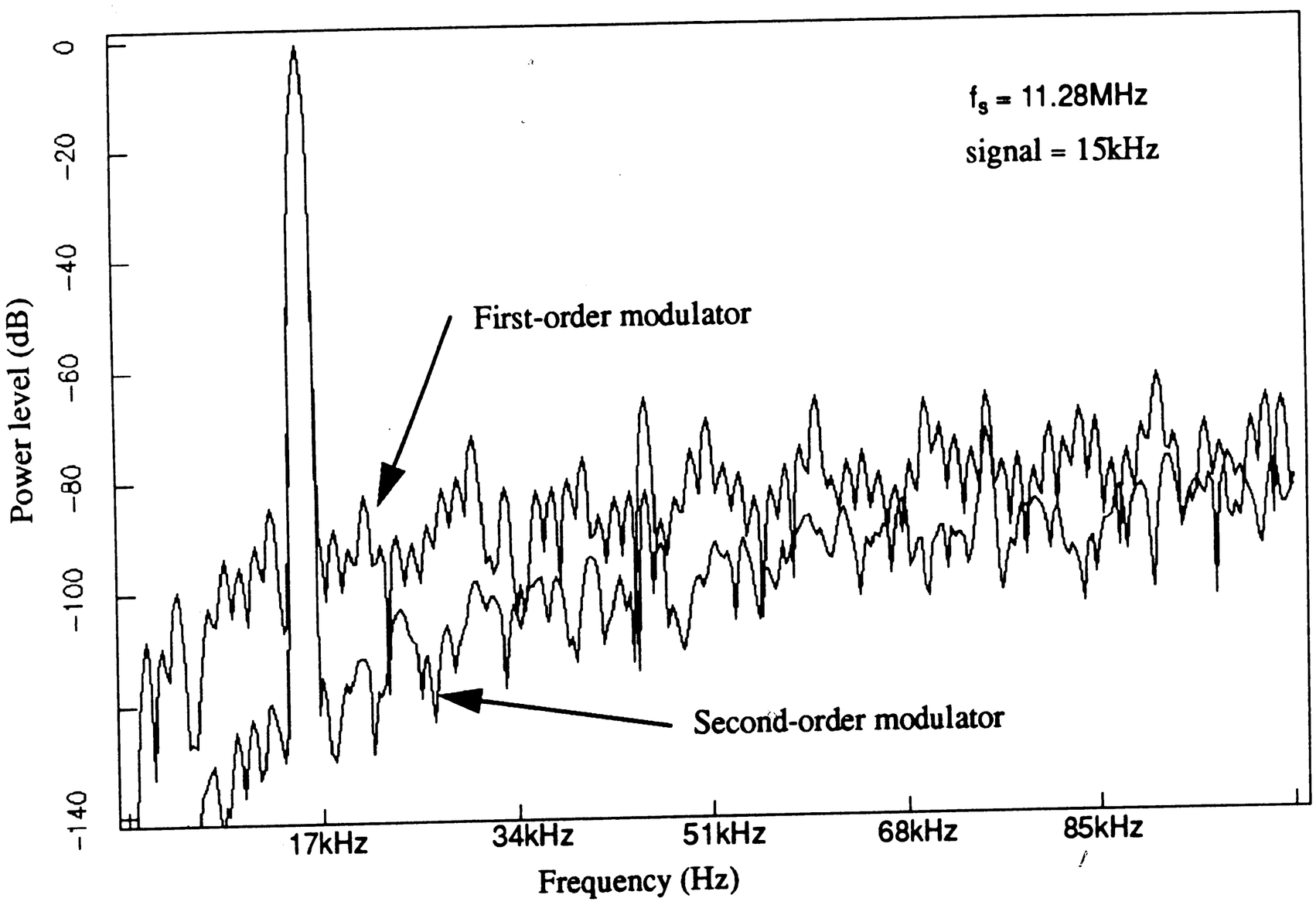
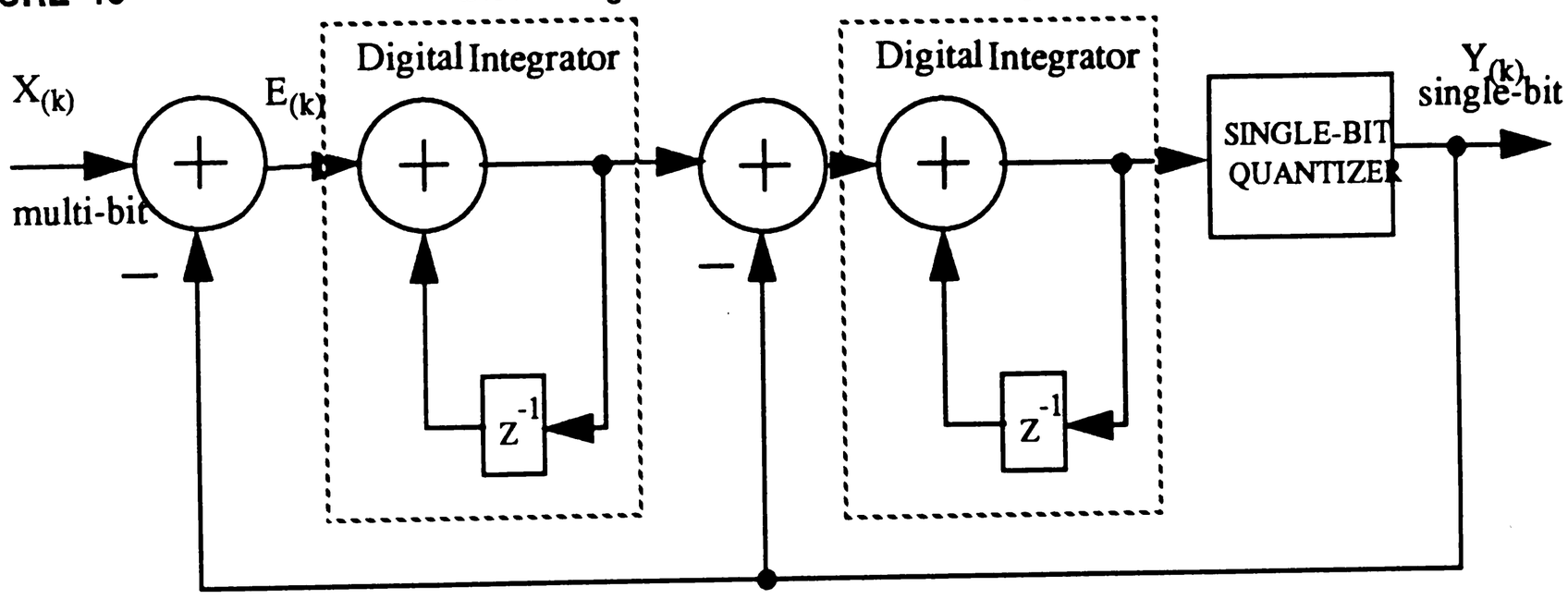


FIGURE 9 shows the modulator output spectrum for the low frequency region near the baseband. Note that the quantization noise level is suppressed by about 100dB in the 0-20kHz region. For comparison purposes, also shown in FIGURE 9 is the baseband spectrum for a second-order Sigma-Delta modulator, note that its baseband quantization noise is suppressed even more than the first-order modulator. Also note that the input signal to the modulator is observable and that the modulator has not introduced and significant harmonic distortion although harmonics do appear to be present. Shown in FIGURE 10 is the architecture for the Second-Order Modualtor. Other architectures can suppress the quantization noise even more and/or delay the frequency at which this noise power starts rising rapidly.

FIGURE 10 Block Diagram of a Second-Order Sigma-Delta Modulator



Another property of Sigma-Delta modulators is that the quantization noise frequency spectra can be scaled. In other words, the shape of the quantization noise spectrum shown in FIGURE 8 (ignoring the signal component) would stay the same, but the frequency axis would be scaled, as the modulator operating speed is changed. For example if the modulator operating speed were halved, the frequency at each tic mark in FIGURE 8 also would need to be halved for the correct spectrum to be shown. Thus lowering conversion speed will have a detrimental effect on the baseband noise level since a greater percentage of the entire spectrum is then used for the baseband signal. This is also know as the over-sampling ratio, which can be defined as the ratio between the modulator operating frequency and the maximum input signal frequency. Typically for each doubling of the over-sampling ratio, the signal to quantization ratio in the baseband can be improved by 6dB.

1.3.2 Some Sigma-Delta Modulator Concerns

Pattern noise, or tones as they are sometimes known, can be generated by Sigma-Delta modulators [4], [5] when converting signals of certain specific fixed amplitudes. This type of noise is more prevalent in certain Sigma-Delta architectures, most notably first-order modulator loops with an input level near the center or either end of the input range. Because the modulator generates its output by switching between two fixed reference levels (-1,+1), at particular input amplitudes, the modulator produces repetitive patterns of 1-bit output data. For example with an input signal slightly above or below the center of the input range, the modulator will produce an output pattern with alternating outputs (i.e. 101010...)

with an extra ±1 breaking the pattern in a repetitive manner . Thus when averaged, the output produces the correct amplitude, but since the extra ±1 occurs repetitively , produces a repetitive output pattern. If the period of this pattern happens to fall within the baseband, then an audible tone will be produced. The tendency of a modualtor to produce pattern noise depend upon its architecture. Another method to reduce pattern noise is the introduction of a dither signal to the data being converted.

A dither signal can be either a random or repetitive pattern of small amplitude with frequency components lying outside the baseband. By introducing dither, the input to the modulator constantly varies, effectively preventing the formation of audible pattern noise. Since the dither signal contains only out-of-band energy, it does not affect the audio output and can easily be removed by the analog lowpass post-filtering.

Stability of the modulator is a major concern when choosing a Sigma-Delta modulator architecture. If the modulator becomes unstable, the output is not an accurate representation of the input signal. Thus until the modulator recovers, the output will be distorted. Most notably stability is a problem with third-order or greater modulators [2,5,6] unless a suitable architecture is chosen.

1.4 Some Conceptual Ideas About Filtering and Switched-Capacitor Circuits

In order to develope the main topic of this thesis, it is first necessary to understand some initial concepts about filtering and switched-capacitor circuits. These concepts will be discussed in the following sections.

1.4.1 What is Filtering

Filtering [9] is the process of altering the frequency domain and time domain characteristics of a signal. In the case of Sigma-Delta modulation, a lowpass filter is needed to attenuated the quantization noise energy above the baseband. Mathematically filtering can be represented as multiplication in the frequency domain:

$$Y(s) = X(s)\,H(s) \qquad \text{(EQ 2)}$$

where X*(s)* is the filter input spectrum, *Y(s)* is the filter output spectrum and *H(s)* is the filter transfer function. Since Sigma-Delta modulators have a quantization noise energy spectrum that increases rapidly with increasing frequency, the required post-filter must have an amplitude response with a sharp cutoff. For a digital audio quality system, the post-filter should have a constant amplitude response and linear phase response. For example the amplitude response is typically specified to be constant within 0.02dB over the entire baseband. To achieve this level of performance from an analog filter is difficult, often requiring the use of precision matched components, wide bandwidth opamps and hand tuning during the initial manufacturing. Due to the difficulties in manufacturing analog filters, digital filters have become popular since the filters performance is determined by stored coeficients. These coefficients if stored digitally cannot change or if stored in an analog manner change very little. In either case a digital filter is not to sensitive to errors in these coefficients.

1.4.2 FIR Filtering and Determining Frequency Response

Digital FIR filters operate on the basic property that multiplication in the frequency domain is equivalent to convolution (multiplication and accumulation) in the time domain[10]. For filtering to be accomplished, the impulse response sequence (of the desired frequency response) is convolved with an input data sequence. Given a desired frequency response $H_d(e^{j\omega})$, it can be translated into the sampled data domain where it becomes $H_d(\theta)$ and is periodic with a period of 2π. The frequency response can be represented as a Discrete Time Fourier Transform (DTFT)

$$H_d(\theta) = \sum_{k=-\infty}^{\infty} h_d(k)\, e^{-jk\theta} \qquad \text{(EQ 3)}$$

and further translated into an impulse response by:

$$h_d(k) = \frac{1}{2\pi}\int_{\pi}^{\pi} H_d(\theta)\, e^{jk\theta} d\theta \qquad \text{(EQ 4)}$$

Notice that $h_d(k)$ is derived from an integral, thus it is possible for the impulse response be of infinite length. Realizing one must have a finite length N for the impulse response, then what are we compro-

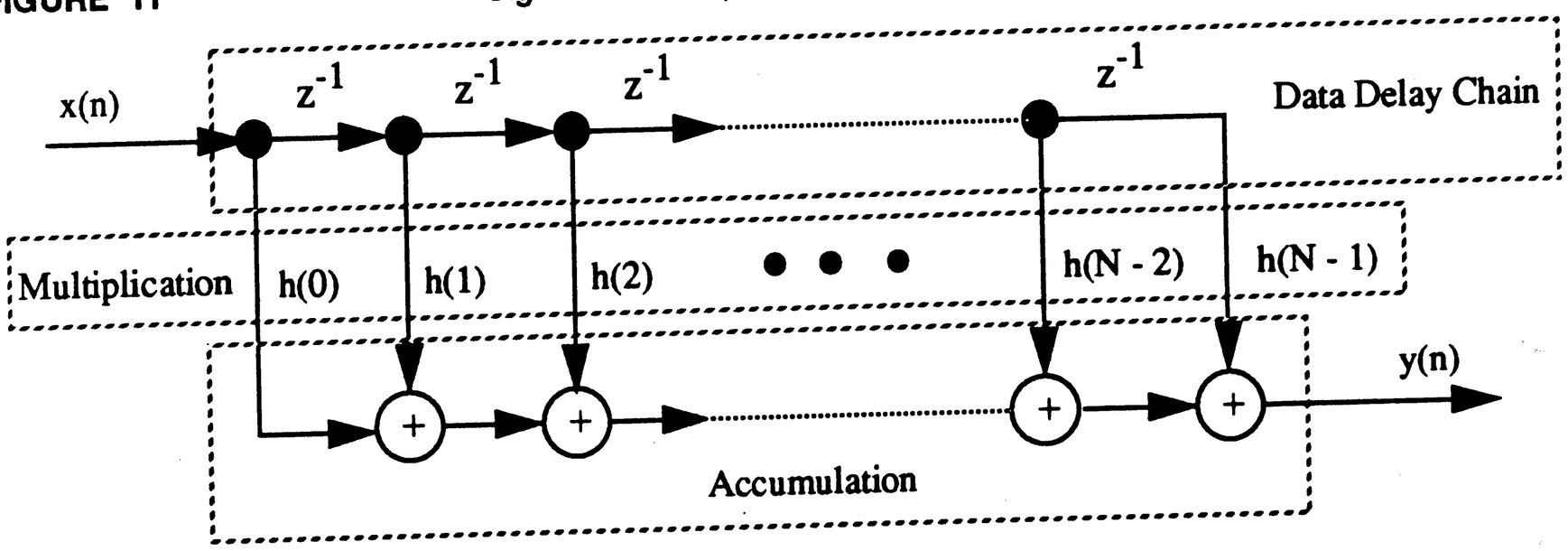
mising? Given that N is finite and knowing that in the discrete time domain frequencies range between $\pm\pi$, then one notices that only a finite number of points from $H_d(\theta)$ may be defined and translated to an impulse response. This is limits the frequency resolution of the FIR filter to $2\pi/N$ determining the minimum frequency bandwidth over which discontinuities in the desired frequency response can be accommodated. Thus when designing a FIR filter, one of the main goals is to determine the minimum impulse response length N which best approximates the frequency response desired.

Having determined the impulse response coeficients, then the actual filtering is accomplished by convolution of $h_d(k)$ and x(n) (the data input sequence) both of which are of length N. Mathematically convolution is defined as

$$y(n) = \sum_{k=0}^{N-1} h_d(k)\, x(n-k) \qquad \text{(EQ 5)}$$

where y(n) is the filtered output. A signal flow graph of the convolution process which gives one a visual representation the filter architecture, is shown in FIGURE 11

FIGURE 11 Signal Flow Graph of the Convolution Process.



For a digital audio DAC in which a Sigma-Delta modulator converts the input to an one-bit wide data stream, a delay chain of simple latches is sufficient to store data length needed for the convolution. Since the data input to the filter is one-bit wide, the multiplication process in FIGURE 11 simplifies to addition where either a particular h(k) coefficient value or zero is accumulated in the convolution. Al-

though during the accumulation process, the digital output word gains significance with a corresponding increase in word length. Thus one would need a multi-bit DAC to convert the output of the FIR filter back into the analog domain.

1.4.3 What is Linear Phase and How is it Related to Symmetry and Area Savings

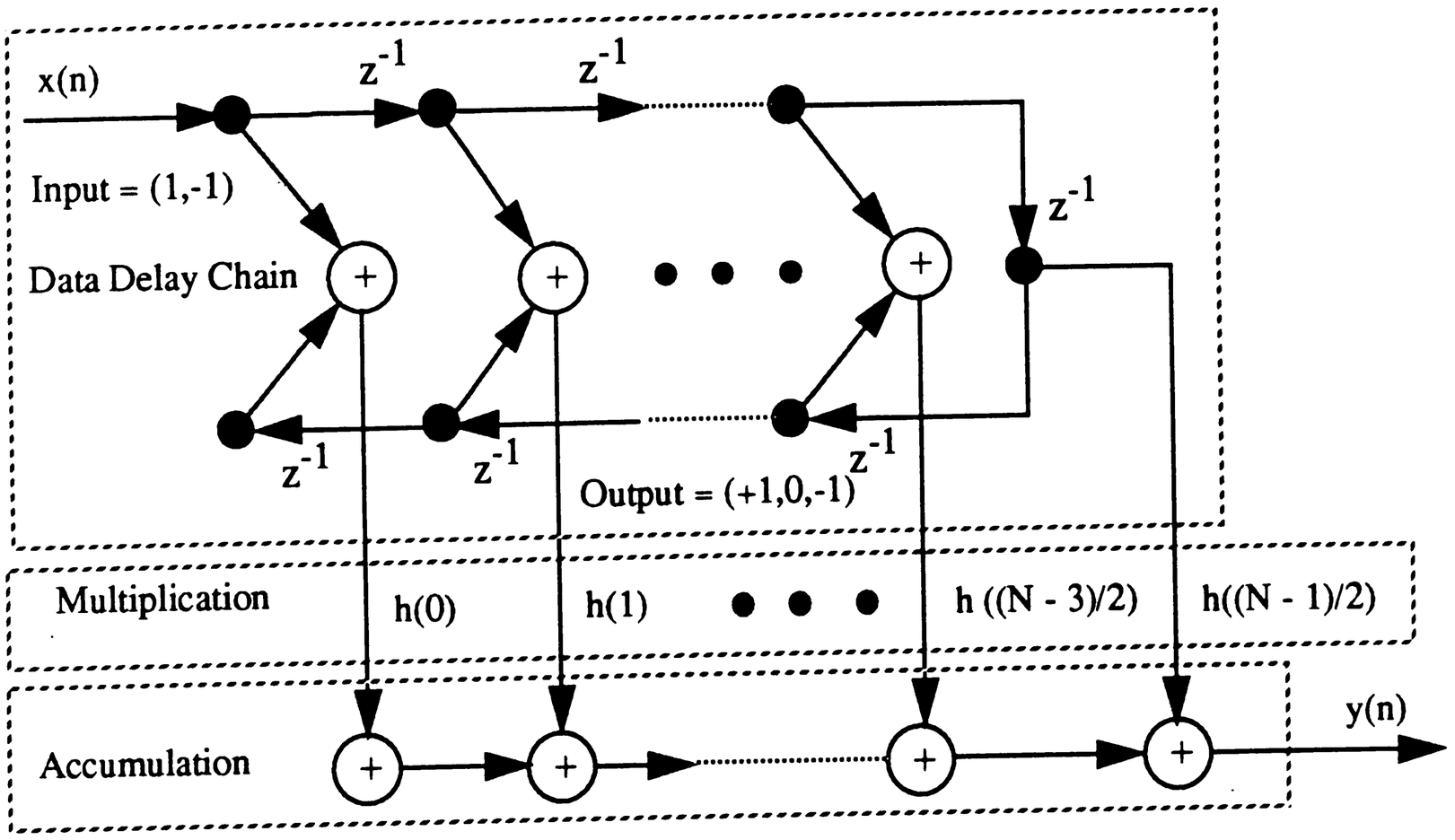
Linear phase [10] in a filter means that a plot of filter phase shift versus frequency is a straight line, thus $\frac{d\phi}{d\omega}$ is a constant. In the time domain, the linear phase property translates into a equal delay of the various signal frequencies passing through the filter. If a filter does not have linear phase, then the phase delay versus frequency plot will not be a straight line and the filter is said to cause phase distortion. When a signal simultaneously containing energy at many frequencies is applied to a non-linear phase filter, the time delay presented to the various frequency components varies and the phase relationships between the various components is altered. For example a step response in the time domain can become rounded as phase distortion occurs. In a digital audio system, phase distortion affects the reproduction of the sound stage (being able to imagine the locations of various sounds relative to one another by listening).

When a filter is designed with a linear phase response, the impulse response sequence takes on an interesting form, becoming symmetrical about its center. Thus for an impulse response sequence of length *N* (where N is odd)

$$h(n) = h(N - 1 - n) \qquad \text{(EQ 6)}$$

causing only *(N+1)/2* impulse response coefficients to be unique. A rearrangement of the signal flow graph presented in FIGURE 11, that takes advantage of symmetry is shown in FIGURE 12. This architecture requires less hardware to implement since the number of multiplications and amount of coefficient storage needed are both halved. This allows the desired system to operate faster and occupy less area than a system not taking advantage of symmetry.

FIGURE 12 Signal Flow Graph of the Linear Phase Convolution Process Taking Advantage of Symmetry Using an Odd Length (*N*) Impulse Response.



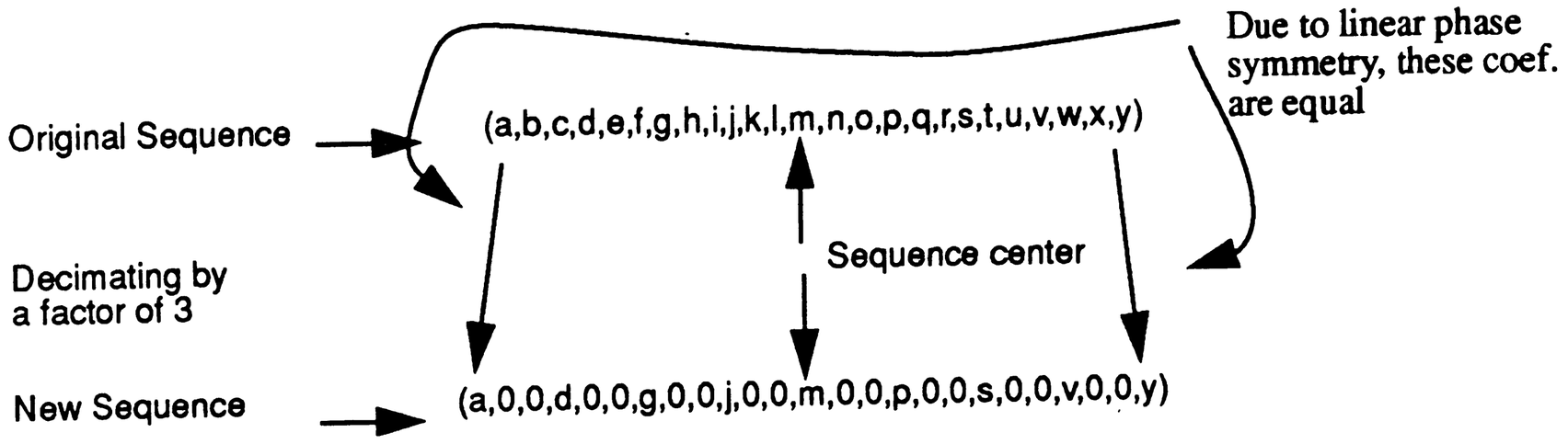
An important difference between these two signal flow graphs is, that in FIGURE 12 two elements from the delay chain are first summed together before they are multiplied by the impulse response coefficient. If the input consists of ±1s, then after the combination of two data samples, the input to the multipliers becomes -2, 0 or 2. Although there are now three possible inputs to the multiplier, the multiplication is still able to be simplified into addition. For this to occur, the accumulator needs to include either the coefficient value, its inverse or zero in the summation. Thus the multiplication has been eliminated by making the accumulation process a little more complex. Each stage in the accumulator of FIGURE 12 needs to make a choice of one out of three possible values to include in the summation. In comparison, each stage in the accumulator of FIGURE 11 needs to make a choice of one out of two possible values. A further discussion on the linearity impact of the third level will be presented in section 3.2.2 on page 42.

1.4.4 Impulse Response Decimation and Comb Filters

Suppose a FIR filter with a length N was designed with a lowpass characteristic. Next suppose that the impulse response sequence is broken into groups of length M and that the one member of each

group retains its original value and the remaining coeficients are set to zero. This is called impulse response decimation[11]. This results in a filter of length N but only has N/M active coefficients in the convolution. Decimation also results in the original passband response being duplicated (M - 1) times evenly spaced throughout the range 0 to 2π. Because of these repeated passbands, a filter with this characteristic is sometimes called a comb filter, since a plot of amplitude response versus frequency resembles the repetitive pattern of teeth on a comb. If these coefficients are stored as capacitor values and coefficient symmetry is used, then only N/2M capacitors are needed. This decimation process is graphically depicted in FIGURE 13

FIGURE 13 Impulse Response Decimation of an Odd Length Sequence



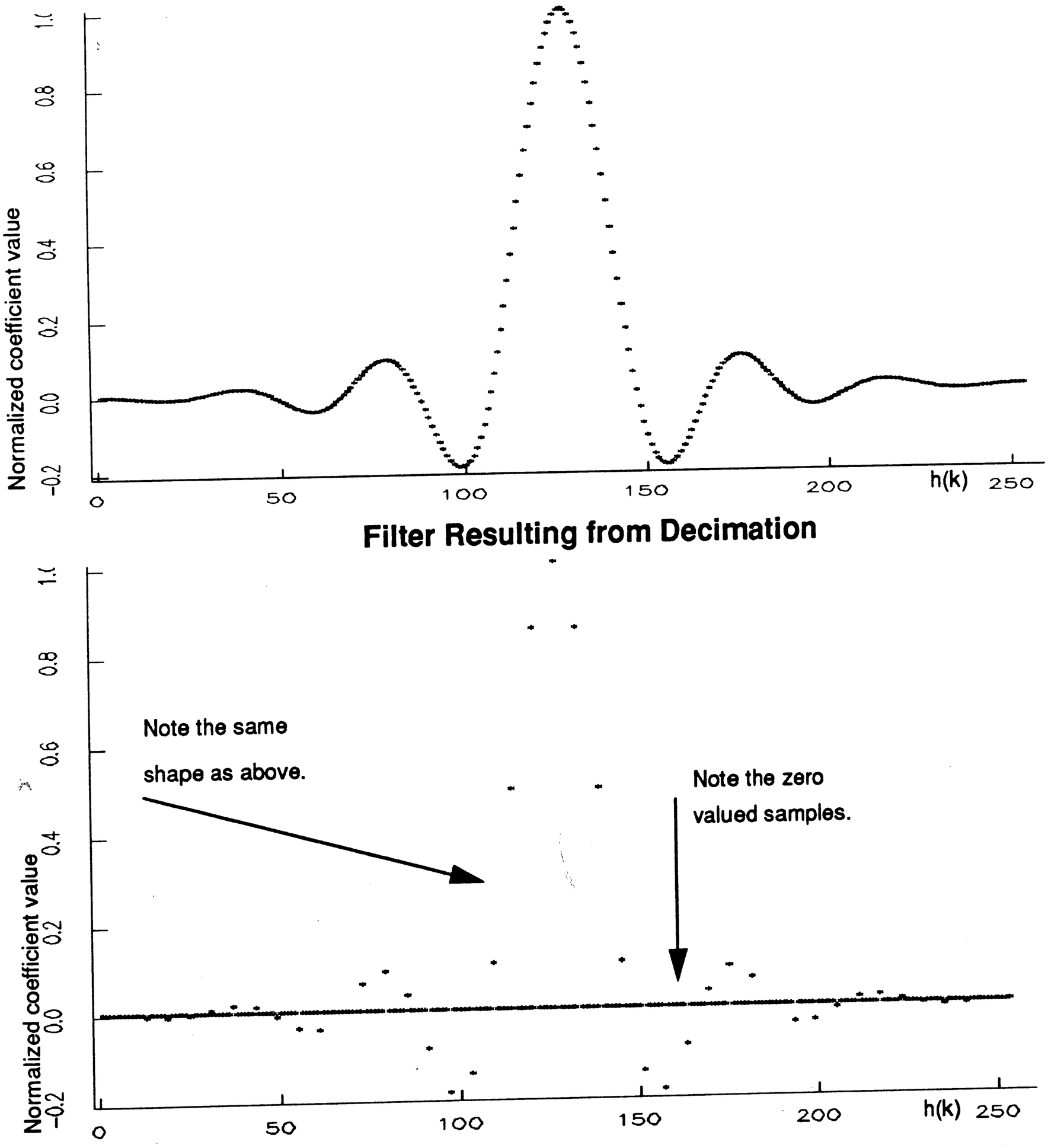
Note that the sequence length N must be such that --> mod (N / 2M) = 1

To demonstrate the properties of comb filters, lets observe the impulse response sequence and frequency response for a FIR filter and a decimated version of that same filter. To properly choose the filter length N, one first must know the desired decimation factor M, since for an odd length filter an integer number of M-length groups plus the center sample must compose the impulse response. This suggests the following relation:

$$mod\left(\frac{N}{2M}\right) = 1 \qquad \text{(EQ 7)}$$

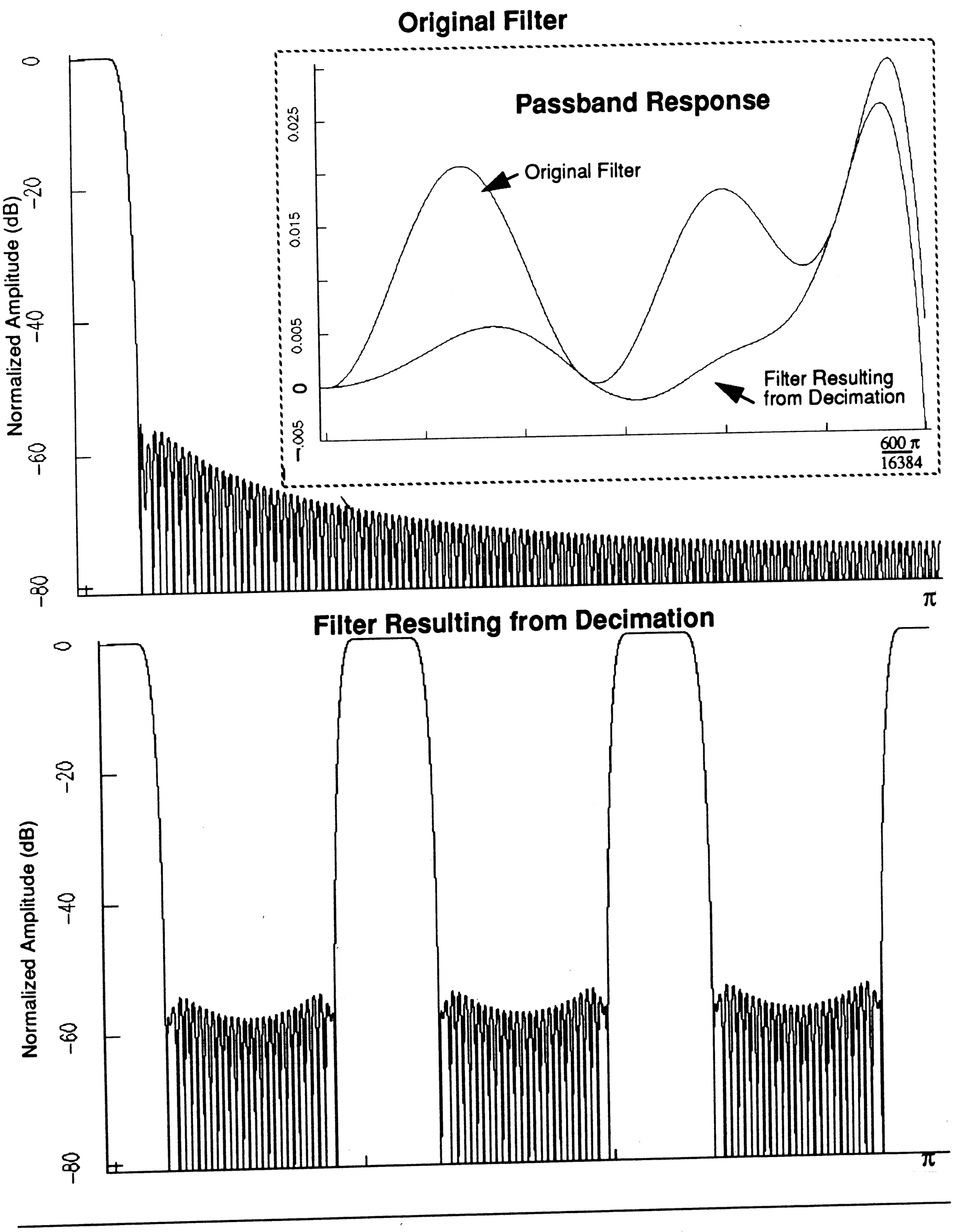
Thus if the desired decimation factor is 6, and the desired filter length is somewhere near 255, then N must be chosen to be 253. For the purposes of this section, an IEEE program [19] which generates FIR filter coeficients was used to obtain the impulse response coefficients for a lowpass filter with N=253 and θ_c=0.025 (this is a normalized value ranging from 0 to 1 corresponding to the discrete time frequency range 0 to 2π) using a Kaiser window. These coefficients were then decimated such that only 43 of the original 253 taps remain non-zero. FIGURE 14 shows plots of the impulse response coefficients for both filters.

FIGURE 14 Impulse Responses for the Original and Decimated FIR FIlters



By performing an FFT on these coefficients, the frequency response of the filter can be obtained as shown in FIGURE 15 Note that the number of repeated passbands is equal to the M-1.

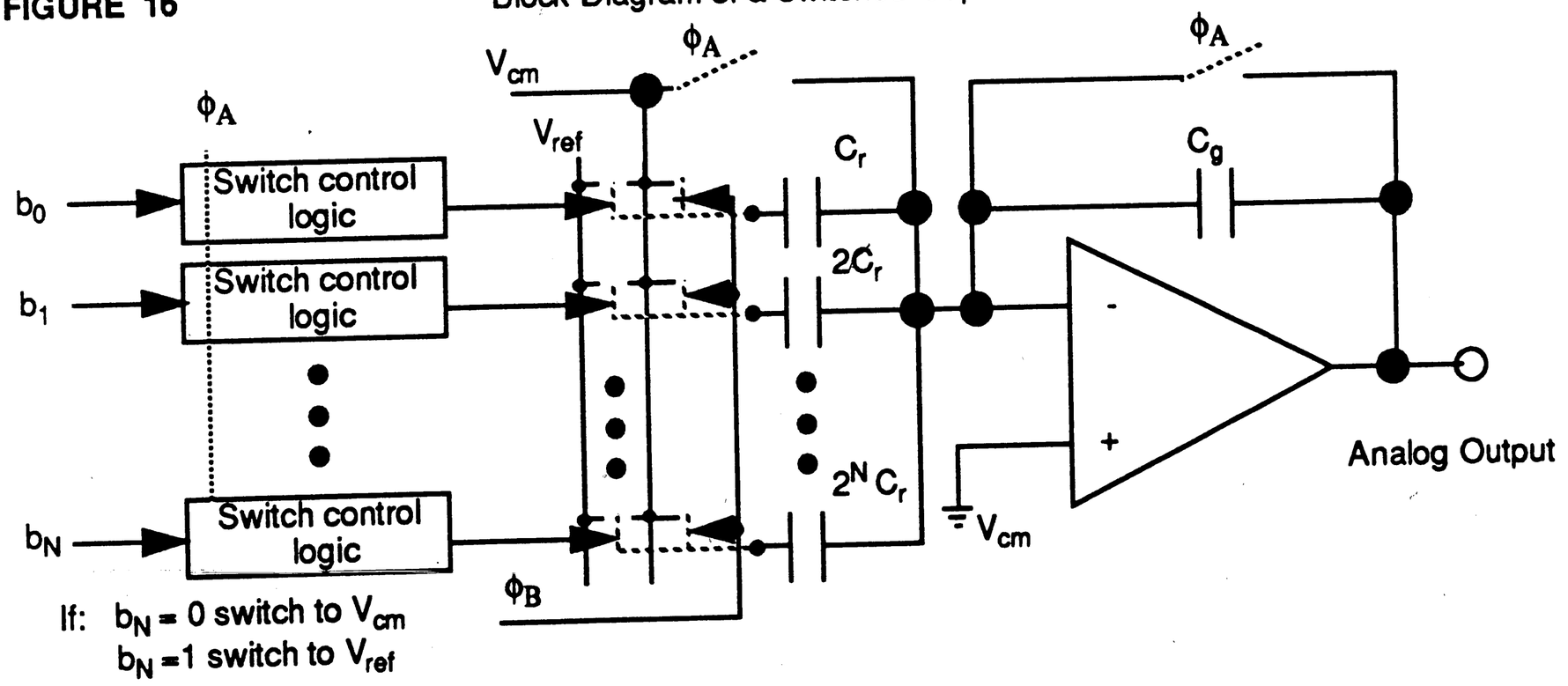
FIGURE 15 Frequency Spectrums for the Original and Decimated Filters



1.4.5 What is a Switched-Capacitor DAC

A Switched-Capacitor DAC (SC-DAC), is a Digital to Analog converter whose output steps are determined by the charge stored upon capacitors. If one uses a typical binary weighted DAC as an example, then an array of capacitors are needed, one for each bit of the input, with the LSB capacitor being the smallest value (C_r) and the remaining capacitors each increasing by $2^N(C_r)$. The conversion process thus converts the input code into a proportional charge stored in the capacitor array. These individual charges are then summed together and transferred into another capacitor to develop an output voltage proportional to the input code. Since in IC technologies, capacitors can be made that match one another to within 0.1%, the untrimmed converter linearity is limited to about 10-bits. In other words any mismatches between the capacitor ratios results in non-linearity and harmonic distortion. It is important to note that with a binary weighted converter, the spread in capacitance values needed for the weighted array is equal to 2^{N-1}. Thus a 10-bit converter would require a ratio of 512 between the largest and smallest capacitors. If the smallest capacitor value is 0.5pF then the largest would be 256pF for a total of 511pF for the input capacitor array. Including the summing capacitor, which is typically equal in value to the MSB capacitor for unity gain, then a total of 767pF are required to build the DAC. FIGURE 16 shows a block diagram of a SC-DAC.

FIGURE 16 Block Diagram of a Switched-Capacitor DAC



This converter is controlled by a two phase non-overlapping clock (ϕ_A and ϕ_B). During ϕ_A, the gain setting feedback capacitor C_g is shorted to the common-mode voltage V_{cm} along with the bottom-plates of the weighted capacitors. Also during ϕ_A, the top-plates of the weighted capacitors are selectively either charged to the common-mode voltage if that bit position data was a "0" or to a reference voltage V_{ref} if the input data bit was a "1". By the end of ϕ_A each of the N weighted capacitors either has no charge stored on it or a charge proportional to 2^N where N is the bit-position for that capacitor. In addition at the end of ϕ_A the total charge stored on the array is proportional to the input code. During ϕ_B, all the capacitor top plates are switch to V_{ref} and C_g is connected in the negative feedback loop. As a result, charge stored on the weighted capacitor array is transferred into C_g where it produces an output voltage. that is dependent upon the total charge stored in the capacitor array.

In summary a SC-DAC uses the principles of charge storage, summation and transfer to accomplish D/A conversion. The linearity of this type of DAC is determined by the matching of capacitor ratios. As stated before, capacitors in IC technologies match within 0.1% or about 10-bits of linearity. For Digital-Audio applications 16-bits of linearity and resolution are required.

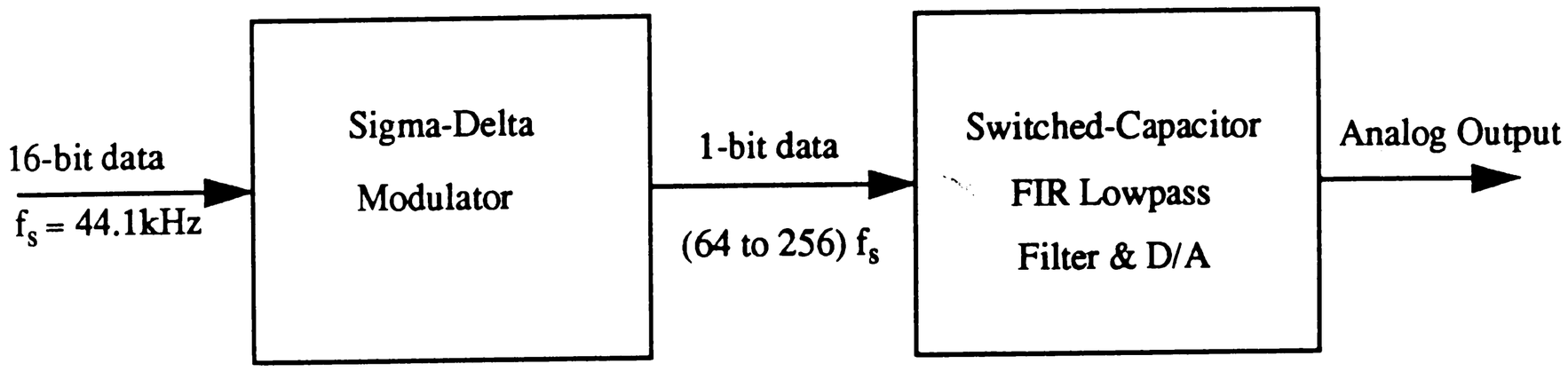
1.4.6 How Can a SC-DAC be a FIR Filter

Remembering that Sigma-Delta modulation can produce a 1-bit wide representation of a signal at a rate many times the Nyquist rate and that a FIR filter operates by convolving a sequence of past input samples with impulse response weights, then one could imagine a system in which the 1-bit data output from the Sigma-Delta modulator could be the input data to the FIR filter. The FIR filter convolution is simplified into addition (charge accumulation) since the input data, when symmetry is used, takes on only the integer values of +1, 0 or -1. The frequency response of the FIR filter is determined by impulse response weights used in the convolution and can be implemented as a series of capacitors proportional to the impulse response weights.

It is important to note that for a FIR filter, errors in the impulse response coefficients as set by the capacitor values do not generate harmonic distortion but instead slightly alter the frequency response. The most notable affect to the frequency response is a reduction of the ultimate stopband attenuation.

The reason errors in the impulse response coefficients do not produce harmonic distortion is that convolution is a linear process.

FIGURE 17 Block Diagram of a Digital Audio System Based Upon a SC-DAC



Shown in FIGURE 17 is a block diagram of a digital audio SC-DAC[20]. The digital audio signal is first converted to a one-bit signal at many times the original sampling rate by the Sigma-Delta modulator. This one-bit signal is then shifted through a digital shift register which has a length equal to the FIR filter length. The analog output is then generated from the convolution of the stored one-bit data output and the FIR filter impulse response coefficients.

1.5 Organization of this Thesis

This thesis is organized into four major chapters which are:

1. Introduction and Background Theory on page 2.
2. The State of the Art on page 26.
3. The FIR DAC Architecture on page 34.
4. Conclusions and Future Work on page 47.

The introduction chapter presents an overview of the information to be presented in the thesis and a background on digital audio, Sigma-Delta modulation, FIR filtering and Switched-Capacitor circuits.

Chapter 2 presents brief discussions of two currently employed Sigma-Delta based DAC architectures are presented. These discussions will include circuit topology, advantages and disadvantages. Also presented is a paper discussing a Switched-Capacitor (SC) Finite Impulse Response (FIR) filter.

Chapter 3 will discuss in detail how the FIR filter is incorporated into the DAC structure. Also discussed will be the needed specifications for the FIR filter such as impulse response length and the desired frequency response. Other topics to be covered include the required three-level DAC linearity and opamp gain.

Finally Chapter 4 will summarize the major design points of the preceding sections with emphasis on the new aspects of combining the DAC and the FIR lowpass filter. Also presented will be some suggestions for further work and acknowledgments.

2.0 The State of the Art

The next sections will present an overview of two current state of the art Sigma-Delta based DACs and a FIR filter realized in a switched-capacitor architecture. Each section discusses the basic system architecture, advantages, disadvantages and performance. Presented are:

1. A CMOS Stereo 16-bit DAC for Digital Audio [11].
2. 17-bit Oversampling D/A Conversion Technology using Multistage Noise Shaping (MASH) [6].
3. Switched-Capacitor Realization of FIR Filters. [12]

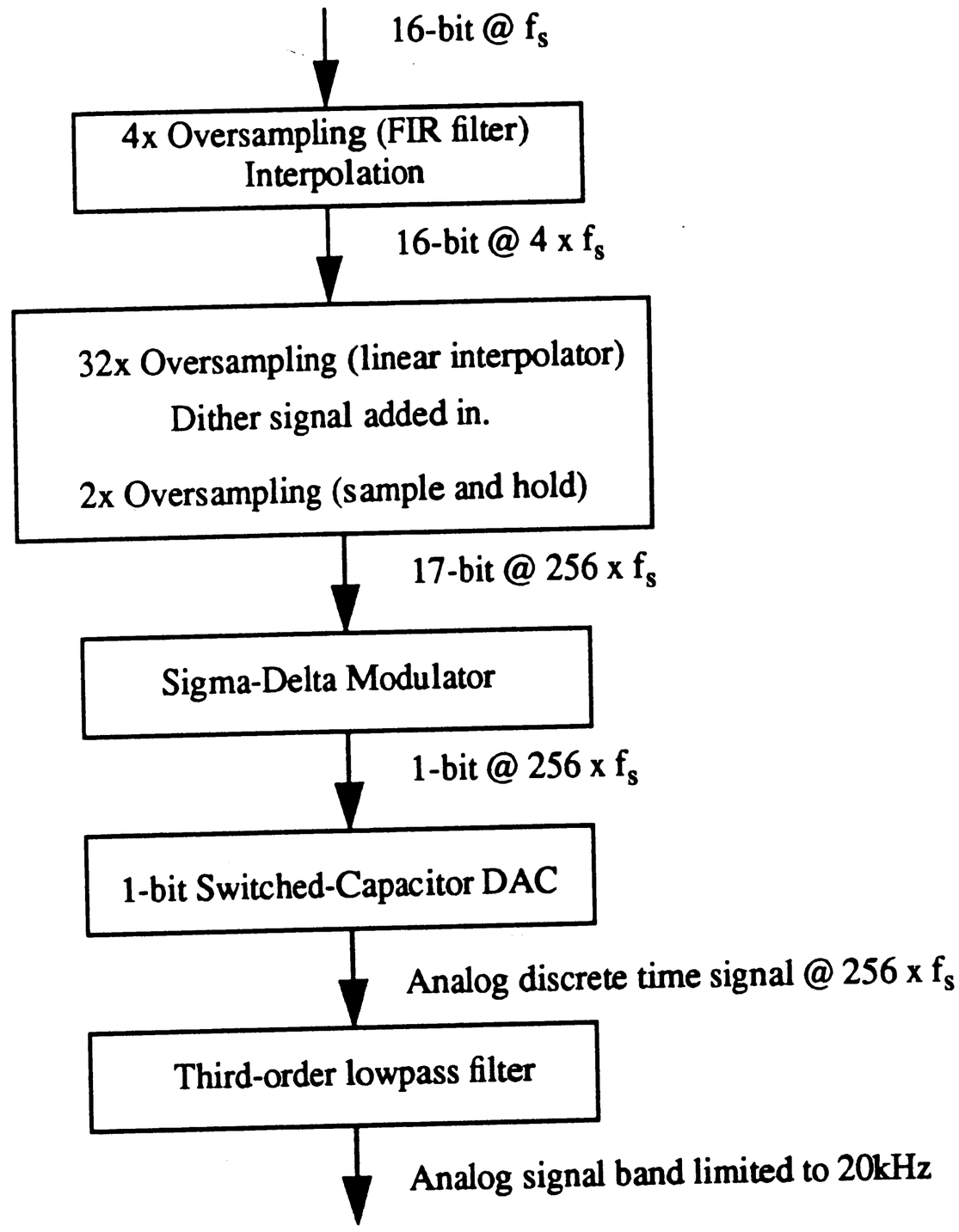
2.1 A CMOS Stereo 16-bit DAC for Digital Audio

This converter [11], one of the first to use the Sigma-Delta modulation technique for audio D/A conversion, was designed by Phillips Research Labs and described in 1987. This is the first publication I could find that used Sigma-Delta modulation for high performance D/A conversion. They were able to obtain a dynamic range of 94dB with a Signal to (Noise + Distortion) Ratio of 90dB.

2.1.1 The System Architecture

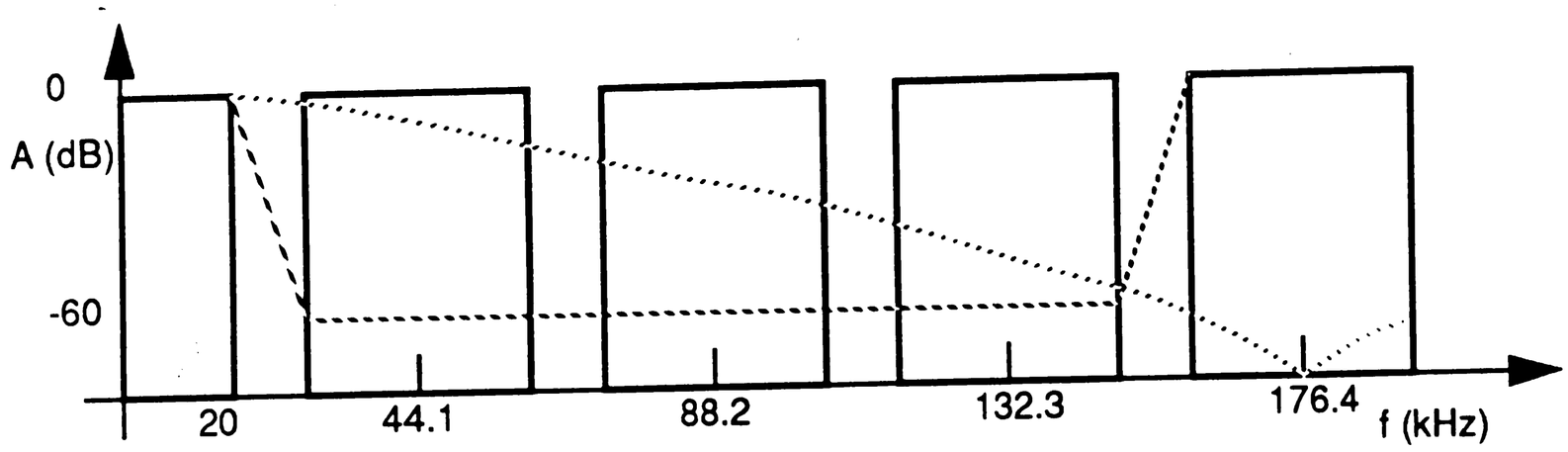
The Phillips converter consists of three stages of oversampling followed by the Sigma-Delta modulator and a 1-bit Switched-Capacitor DAC (SC-DAC). The SC-DAC also contains a first-order lowpass filter and is followed by a second-order Butterworth lowpass output filter. The block diagram is shown in FIGURE 18

FIGURE 18 Functional Block Diagram of the Phillips DAC



It is interesting to observe the frequency spectrum as the input signal is passed through the oversampling stages and into the Sigma-Delta modulator. FIGURE 19 shows the spectrums from the first two stages of oversampling.

FIGURE 19 Frequency spectrum of the oversampling filters



——— Baseband input to 20kHz, and resulting images from 44.1kHz sampling

- - - - - - - - - - - - - - First oversampling filter

. . . . . Second oversampling filter $\left(\frac{\sin x}{x}\right)^2$

The first oversampling filter is an FIR lowpass design. It increases the data rate four times and also pre-distorts the signal such that, after passing through the rest of the system, the frequency response is flat within 0.02dB. The input signal is lowpass filtered to attenuate the first three image frequency bands of 44.1kHz $\pm$ 20kHz, 88.2kHz $\pm$ 20kHz and 132.3kHz $\pm$ 20kHz, which are a result of the original 44.1kHz sampling rate. The result is to ease the requirements needed for the analog output lowpass reconstruction filter, since the amount of energy in the 24kHz to 156.4kHz range is reduced by 60 dB by the first stage oversampling filter. If this filter were not present, an output filter with a sharper cutoff and narrower bandwidth would be needed.

The second oversampling filter is a linear interpolator, which further increases the data rate by a factor of 32. The filter is based on an adder structure and has a linear ramp impulse response, which gives rise to its frequency response shape of $sinc^2$. After this filter, an out-of-band dither signal is added to the data to prevent the generation of audible pattern noise. The addition of the dither caused the dynamic range of the signal to be increased by one bit such that the following stages must be 17-bits wide.

The third and final stage of oversampling consists of a sample and hold, which doubles the data rate for a total oversampling ratio of 256. This data is then input into the second-order Sigma-Delta modulator where the 17-bit 256 f_s data is converted to 1-bit data at the same rate. The quantization noise fre-

quency spectrum of the modulator is shaped by the loop feedback to suppress the quantization noise from dc to 20kHz. The 1-bit stream is then used to drive the integrating switched-capacitor DAC where the input is used to determine whether a unit charge is supplied or removed from the integrator. The DAC also serves as a first-order lowpass filter. The signal is then applied to a second-order butterworth lowpass filter with a -3dB frequency of 60kHz.

2.1.2 Advantages, Disadvantages and Performance

The Phillips converter has the following advantages:

1. The DAC linearity is not limited by matching.

Due to the lowpass characteristic of the first oversampling filter, image energy due to the original sampling is removed, but the Sigma-Delta modulator still adds noise energy.

The Phillips converter has the following disadvantages:

1. The analog output filter must have a well controlled cutoff frequency to keep in-band variations in the amplitude and phase responses acceptable.
2. The analog output filter with a cutoff of 60kHz will affect the in-band phase response, which is not desirable for high quality audio applications.

The following statements summarize the converters performance:

- 16-bit resolution, 32-48kHz sample rate, clock rate 256 f_s
- 2- channels, 0.02dB passband ripple, > 60dB stopband attenuation
- >94dB dynamic range, <90dB THD + N, >80dB channel separation
- 5V $\pm$ 10% 250mW power supply, -40 to 85 C^o operation

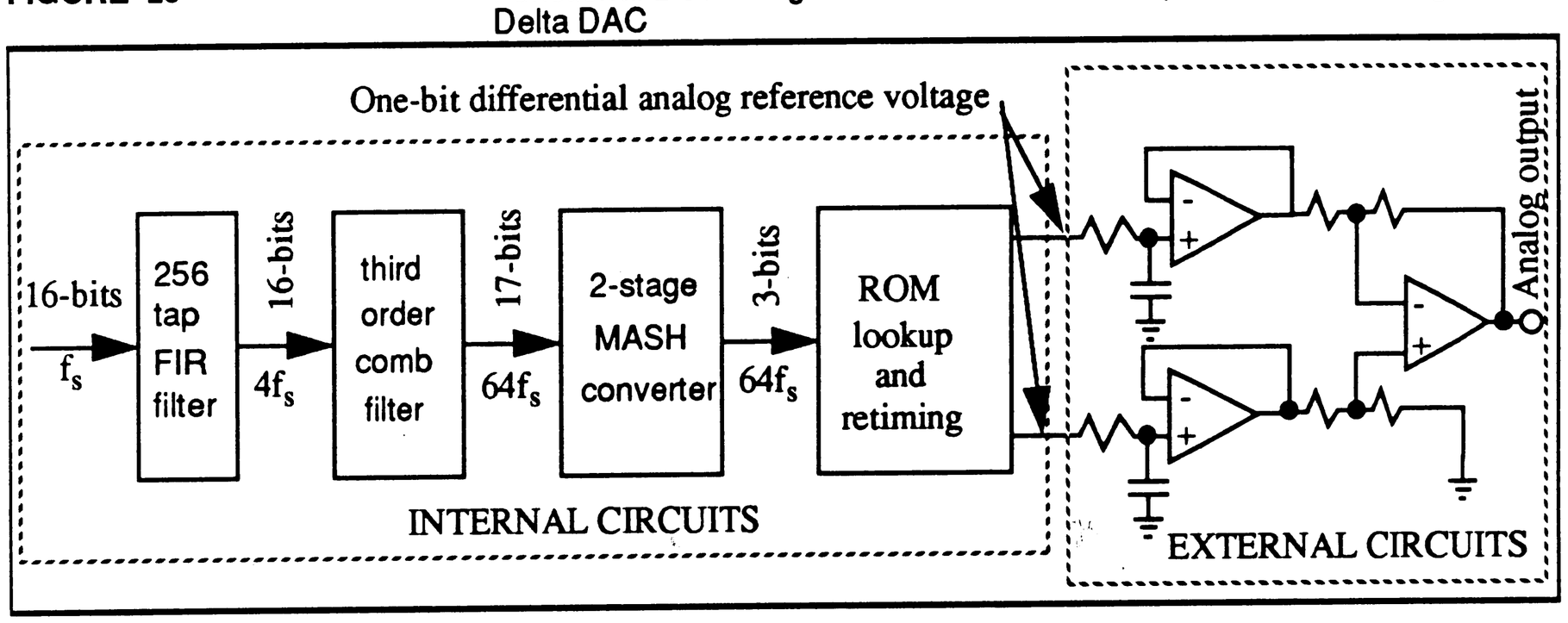
2.2 17-bit Oversampling D/A Conversion Technology using Multistage Noise Shaping

This oversampled Sigma-Delta DAC[6] was designed by NTT in 1988, it has a SNR (S/(N + THD)) of 101dB. In addition to the DAC, presented in this paper and an earlier publication by NTT in 1988 [13] is a description of second-order modulators versus multistage noise shaping modulators. The input to this converter is 16-bit data increasing to 17-bits only after oversampling. Thus the converter does not have 17-bit resolution, as claimed.

2.2.1 The System Architecture

The NTT converter consists of two stages of oversampling followed by a third-order MASH Sigma-Delta modulator, which then drives a 7-level differential pulse-width modulation DAC. There is no mention of any analog post filtering, but the actual D/A conversion takes place in external opamps, where filtering could be easily introduced. FIGURE 20 shows the system architecture for the NTT converter.

FIGURE 20 Functional Block Diagram of the NTT Oversampled Third-order Sigma-Delta DAC

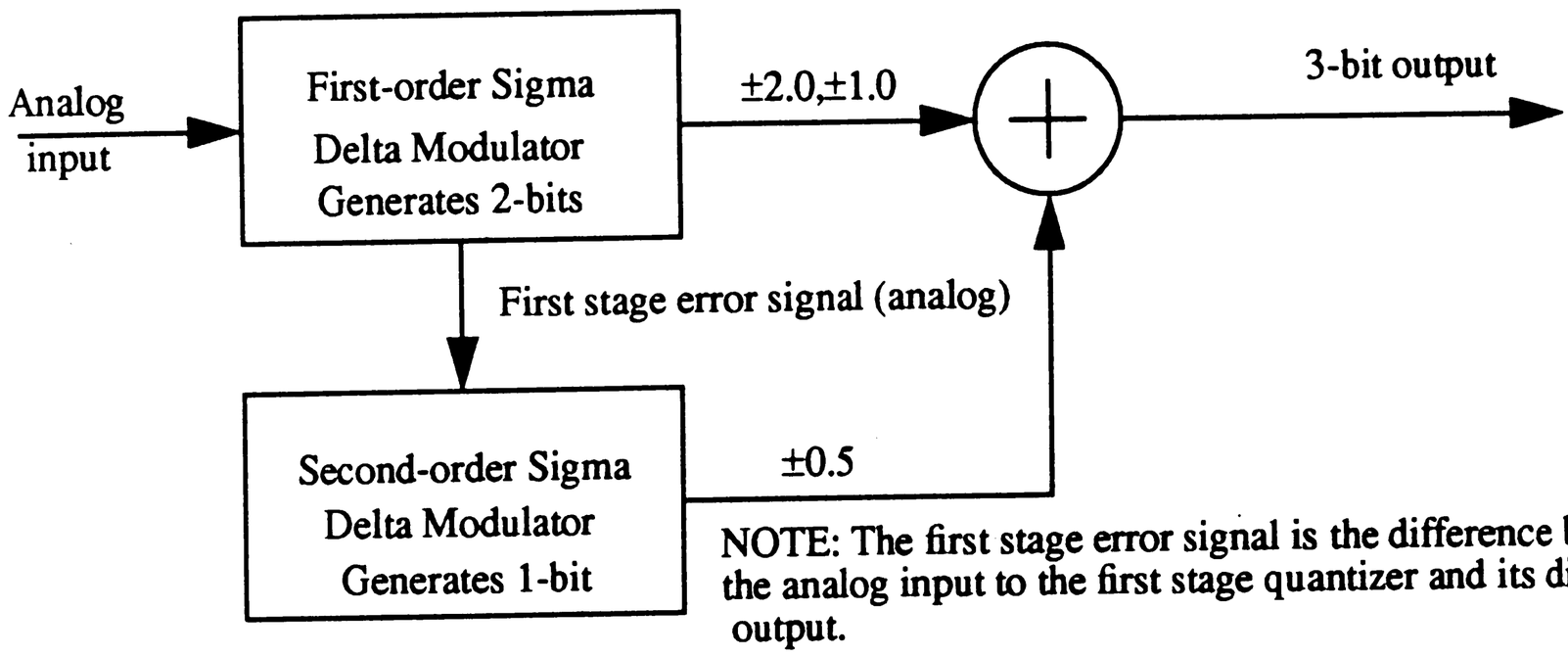


The first oversampling stage, a 256-tap FIR filter, provides a four times increase in sampling rate (presumably also performing a lowpass filter function for the same reasons that the converter from Philips used lowpass filtering). The second oversampling stage provides an additional increase of 16 times for a total oversampling ratio of 64. This filter is a third order comb filter with a 16-bit input word length and a 17-bit output word length, but the paper does not mention why the word length increases, possibly this extra bit could be some type of dithering.

The Sigma-Delta modulator converts the 17-bit data at $64f_s$ into seven quantized levels at $64f_s$ thus requiring the use of a multi-bit DAC since the output is three-bits wide, as shown in FIGURE 21. The third order modulator is composed of a first-order loop in cascade with a second-order loop. In comparison to a second-order modulator, NTT claims that this structure enhances dynamic range, increases stability and further suppresses the modulator quantization noise in the baseband. Combining the effects of

the third-order modulator and its 3-bit output, the required oversampling ratio is less than would be needed for a second-order modulator with a 1-bit output.

FIGURE 21 The NTT MASH Architecture and Resulting Three Bits.



A differential pulse-width modulation output stage (a multi-bit DAC), using the modulator's 3-bit output, selects one of seven patterns stored in ROM to be clocked sequentially into an external differential RC filter. A differential output architecture was chosen to minimize distortion, caused by *on resistance* mismatches between P and N transistors in switches controlling the reference level that is sent to the RC filters. The rate at which data is clocked out of the ROM is unspecified in the paper, but it must be several times the $64f_s$ input rate, since it appears as though the long-term average of the pulses sent to the RC filters determine the analog level produced.

It is interesting to note that the differential pulse-width modulation output stage essentially performs as a Sigma-Delta modulator, in that it trades speed for resolution.

2.2.2 Advantages, Disadvantages and Performance

The NTT converter has the following advantages:

1. The use of lowpass filtering in the first oversampling stage eases the requirements for the analog post filtering.

2. The converter operates with a lower oversampling ratio thereby saving digital switching power.

The NTT converter has the following disadvantages:

1. This part requires the use of three external opamps for the D/A conversion, filtering and differential to single-ended output conversion.
2. External opamps also require power.

The converter has the following performance:

- 16-bit resolution, 48kHz input sampling rate and an oversampling ratio of 64
- 96dB S/(N + THD) ratio, -109dB idle channel noise
- 5 Volt 160mW power (*NOTE:* external opamp power is not included)

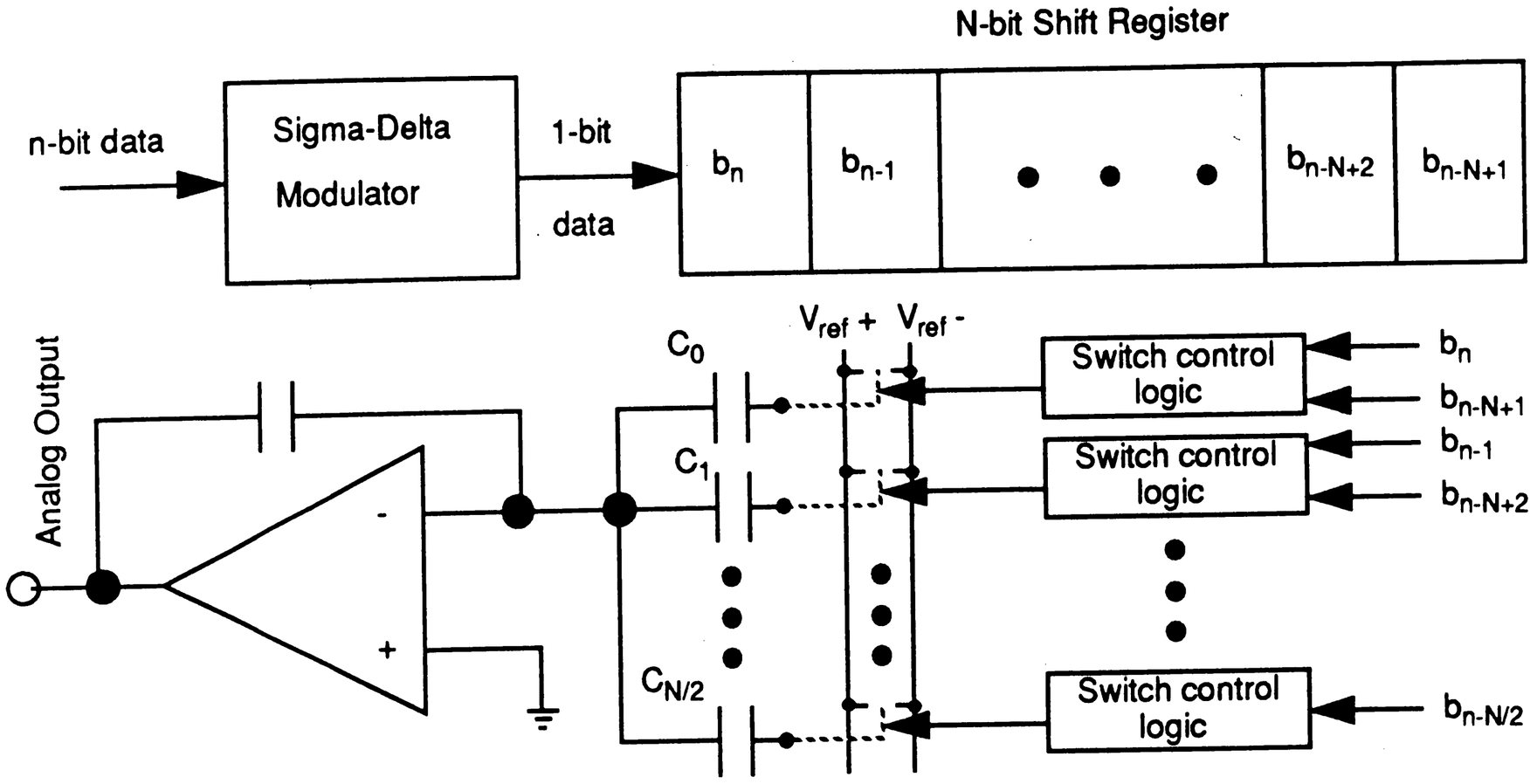
2.3 Switched-Capacitor Realization of FIR Filters

This paper[12] published in 1984 gives a brief description of a FIR filter implemented using a Sigma-Delta modulator and switched-capacitor D/A. Other references of this same nature include [14], [15], [16].

2.3.1 The System Architecture

This system uses a Sigma-Delta modulator to convert incoming multi-bit data into a one-bit stream. The bit stream is then serially shifted through a series of 15 digital delay elements. A FIR filter operates by convolving the delayed data with coefficients representing the impulse response of a filter having the desired frequency response. Typically convolution implies multiplication, requiring a digital multiplier, but since the signal is in a binary form, multiplication is simplified into addition. Taking advantage of coefficient symmetry in a linear-phase FIR filter impulse response, only half of the coefficients are unique, therefore only 8 capacitors are needed to implement a 15-tap filter in a summing switched-capacitor DAC form. The area ratio between these eight capacitors is made the same as the corresponding impulse response ratios. By selecting the appropriate data elements from the delay chain, the switching of each capacitor to the appropriate reference level is determined. Once each capacitor is appropriately switched, the charge of all the capacitors is then summed by the integrating D/A converter. FIGURE 22 shows a block diagram of this filter.

FIGURE 22 Functional Block Diagram for the Switched-Capacitor FIR Filter



Since the data is stored digitally as a *1* or *0* in the delay chain, the filter length can be made long without signal degradation. Signal degradation was a problem in earlier similar designs where the signal was stored in an analog form and repeatedly passed from one delay stage to the next.

2.3.2 Advantages, Disadvantages and Performance

This FIR filter has these advantages:

1. One-bit binary signal storage is useful for generating long signal delays and FIR filters with many taps.
2. As a result of the binary storage, no multiplier is needed. Instead only addition is required which can be accurately performed by the switched-capacitor integrator.
3. Variation of the capacitor ratios due to processing or other factors has very little effect on the inband frequency response of the filter.

This FIR filter has these disadvantages:

1. Care must be taken to minimize the effects of clock feedthrough on the D/A conversion linearity.

No statement of performance was given in this paper other than that the generated frequency response was in good agreement with the desired response.

3.0 The FIR DAC Architecture

This section describes the conceptual architecture for the proposed Switched-Capacitor FIR DAC including the needed specifications for both the FIR filter and operational amplifier (op amp).

There are a number of interrelated design parameters or blocks that control the performance of the proposed DAC architecture. Show in TABLE 1 are the relevant parameters (blocks) and their effect on performance.

TABLE 1 Architectural Parameters and System Performance Effects

PARAMETER or BLOCK	EFFECT
Data rate interpolation and pre-filter.	Sets the spectrum into the modulator and the locations where images of the original sampling rate occur.
Sigma-Delta modulator architecture.	Sets the quantization noise energy in the 0 to 20kHz region and how fast this noise rises with increasing frequency.
FIR filter impulse response shape and length.	Determines the frequency response of the DAC output including baseband response, transition width and stopband attenuation.
FIR filter impulse response decimation factor.	Determines how many of the impulse response coefficients are actually non-zero (active). But causes repeated passbands to occur thereby setting the frequency at which the analog post filter must become effective.
Analog post filter.	Sets limits on the maximum decimation factor and its cutoff frequency location, to limit the effect on the baseband phase and frequency response.

Since this represents a large design space to search for an optimum combination of parameters, only a reduced set of parameters (though not necessarily optimum) will be further considered. Also for simplicity, the pre-filter and sigma-delta modulator blocks will not be described. Where an input is needed for the FIR DAC, it is assumed to come from a second-order sigma-delta modulator.

3.1 The Desired FIR Filter Response

For digital audio (a sampled data system), the frequencies from near DC to 20kHz should be reproduced with as little amplitude and phase response distortions as possible with no energy produced at other frequencies. This defines the ideal desired frequency response $H_d(\theta)$. Because a FIR filter can produce linear phase, a FIR architecture was chosen rather than an IIR architecture. The filter length is chosen to be of odd length N, so that the signal delay caused by the filter is an integer number of clock periods and the center impulse response coefficient is maximum. Ideally one would like the filter to pass all frequencies to 20,000Hz and stop all frequencies above 20,001Hz, remembering back to section 1.4.2 on page 14, this would require a very large N. For example if the D/A conversion rate is 11.28MHz, a filter length N of 11,280,000 is required to achieve a 1Hz cutoff transition. Even if one were to accept a cutoff transition of 20kHz, a filter length of 564 is still needed.

For the proposed architecture, where the charge upon capacitors is summed to form the output, even halving the number of capacitors due to coefficient symmetry, including 282 capacitors in a summation is a difficult task. A method for reducing the number of required capacitors even further is needed. Impulse response decimation, as described in section 1.4.4 on page 17 is used for this purpose. Decimating the impulse response by a factor of M reduces the number of active coefficients from N to N/M + 1. After taking advantage if the linear-phase symmetry, the number of coefficients can be reduced by another factor of two for a total of N/2M + 1 active coeficients. Even though there are a reduced number of coefficients, the sharpness of the cutoff transition and passband response are not affected. Repeated passbands have been created, however.

As a result of the repeated passbands, the DAC output must be analog lowpass filtered to remove the remaining modulator noise and input signal sampling images. This brings about a trade-off between the decimation factor and output filter cutoff frequency. For the output analog filter to remain simple and not to affect the passband amplitude response or linear-phase characteristics, its cutoff frequency should be at least one decade above the upper passband edge. But as the decimation factor is increased, the frequency at which the first repeated passband occurs moves closer to the upper passband edge. With the proper choice of decimation factor and cutoff frequency, however, a near optimum overall fre-

quency and phase response can be obtained. The FIR DAC provides a linear-phase response and a sharp cutoff transition with little processing variation. Then at a frequency about one decade above the pass-band edge, the analog post-filter takes over and reduces the energy present in the repeated FIR filter passbands.

Since the upper passband edge is at 20kHz, the analog post-filter should have its cutoff at 200kHz. For a third-order filter, this results in 42dB of attenuation at 1MHz and 60dB of attenuation at 2MHz. Thus for the repeated passbands to be attenuated sufficiently, they should not occur before 900kHz. This sets the upper limit for the decimation factor at 12 and produces its first repeated passband at 920kHz.

3.1.1 The Proposed FIR Filter Characteristics

The analog filter has imposed some restraints in the FIR filter design but did not determine its length or cutoff frequency. For this digital audio DAC, the passband response should be flat within 0.1dB. This presents some difficulty in determining the cutoff frequency to design into the FIR filter since, usually at the cutoff frequency, the gain is -6dB and the exact gain and ripple in the passband is not known. Also the passband response is slightly affected by filter length along with the transition width.

For these reasons, it was decided to determine the FIR filter coefficients empirically by using the IEEE windowed FIR filter design program. This would allow many combinations of filter lengths and (-6dB) cutoff frequencies to be evaluated for flatness in the 0-20kHz range and transition width. After some experimentation with the various windows available with this program, it was decided to use the Kaiser window exclusively, since it has a flat passband response.

By trial and error, it was determined that a FIR filter of length 817 using a decimation factor of 12 (yielding only 35 active taps) and a normalized (-6dB) cutoff frequency of 0.00385 (43kHz) produces acceptable results. This filter has a passband ripple of less than 0.02dB, which leaves some margin for the analog post-filter. When examining the impulse response coefficients for this filter, it was noticed that the first three and last three tap weights were quite small. Because small variations in the tap

weights are not detrimental to the passband response, the frequency response was evaluated with these tap weights set to zero. Again an acceptable filter response was produced but the filter length has been reduced to 745 with only 32 active taps needed. FIGURE 23 shows a detailed block diagram for implementing the FIR DAC. The frequency response of the FIR filter section is shown in FIGURE 24. The impulse response and normalized coefficients are shown in FIGURE 25

FIGURE 23 Detailed Block Diagram of the FIR DAC

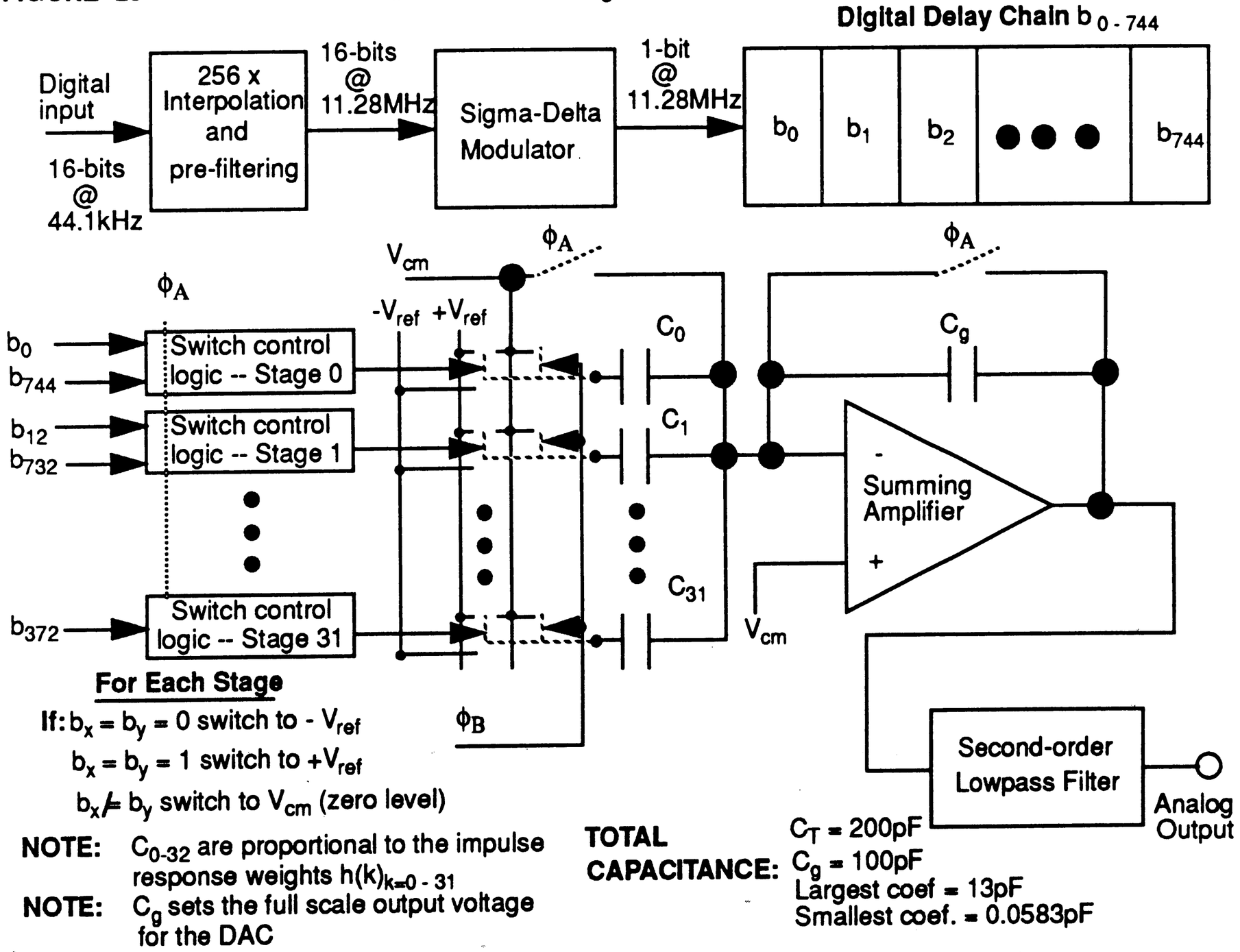


FIGURE 24 Frequency Response of the FIR Filter

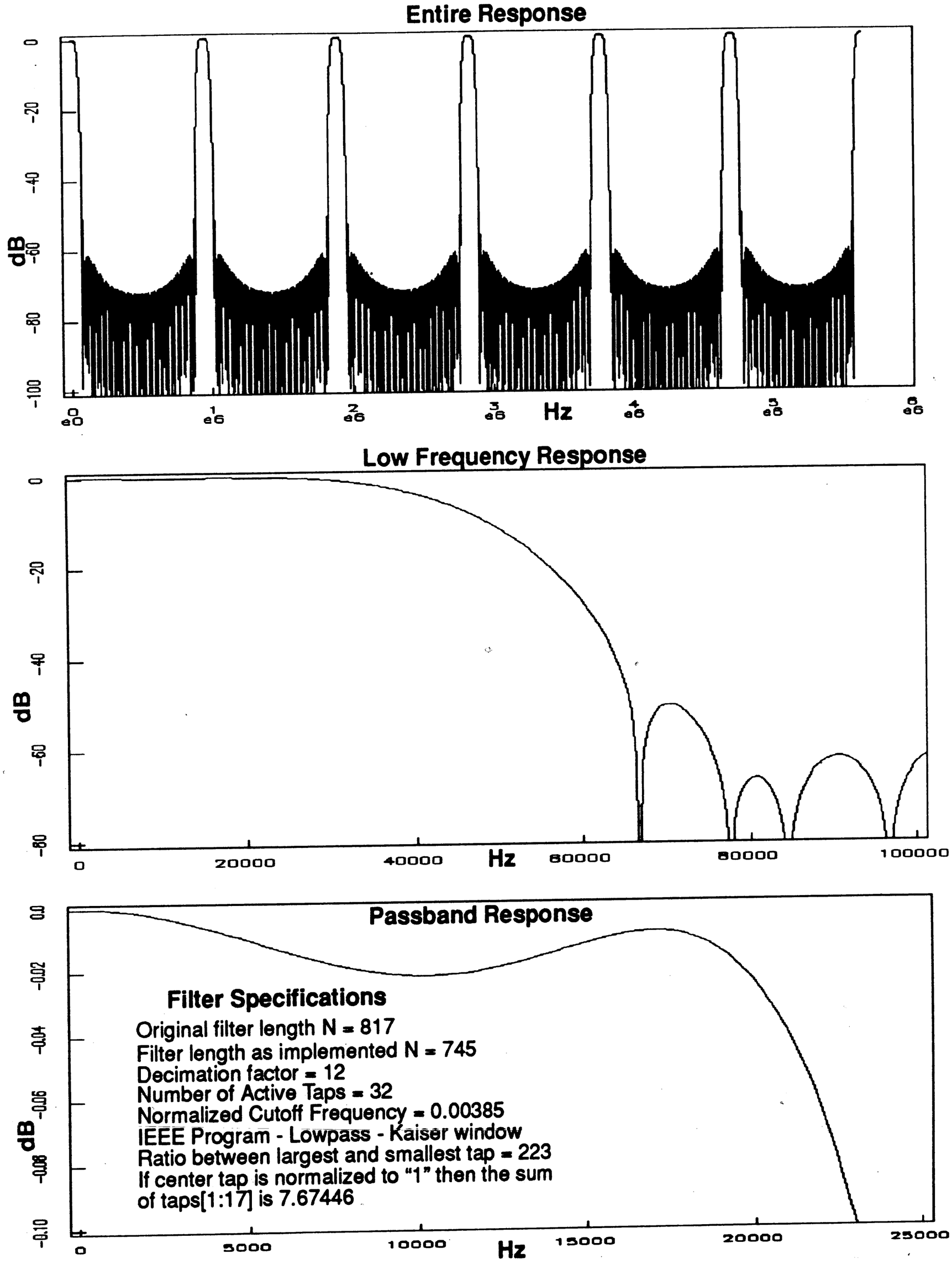
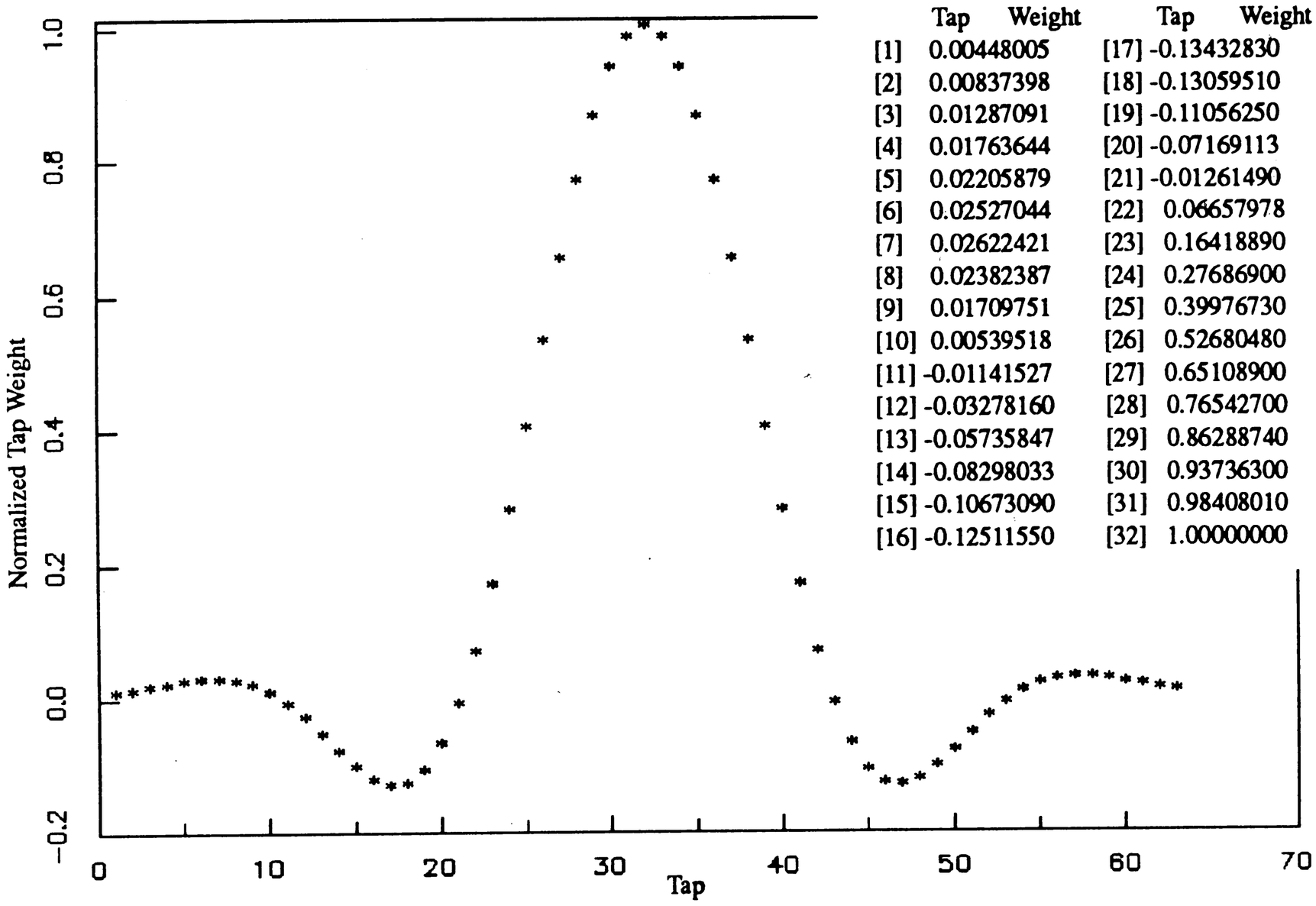


FIGURE 25 Impulse Response of the Designed FIR Filter



	Tap	Weight		Tap	Weight
[1]	0.00448005		[17]	-0.13432830	
[2]	0.00837398		[18]	-0.13059510	
[3]	0.01287091		[19]	-0.11056250	
[4]	0.01763644		[20]	-0.07169113	
[5]	0.02205879		[21]	-0.01261490	
[6]	0.02527044		[22]	0.06657978	
[7]	0.02622421		[23]	0.16418890	
[8]	0.02382387		[24]	0.27686900	
[9]	0.01709751		[25]	0.39976730	
[10]	0.00539518		[26]	0.52680480	
[11]	-0.01141527		[27]	0.65108900	
[12]	-0.03278160		[28]	0.76542700	
[13]	-0.05735847		[29]	0.86288740	
[14]	-0.08298033		[30]	0.93736300	
[15]	-0.10673090		[31]	0.98408010	
[16]	-0.12511550		[32]	1.00000000	

Another important feature of this architecture is that errors in the coefficients as set by the capacitor values do not produce harmonic distortion. This is not the case if the capacitors were used in a binary weighted DAC. Thus when the circuit is laid out, the matching between the capacitors is not very critical. This improves performance and saves area.

To show the effects of combining a Sigma-Delta modulator and decimated FIR filter, a computer simulation was performed in which a sine-wave signal was passed through such a system. Shown in FIGURE 26 is the low frequency spectrum for this system, first showing the modulator output and then the spectrum after FIR filtering. It is interesting to notice that in the 0 to 20kHz range, the spectrums are identical.

FIGURE 26 Baseband Frequency Spectrums at the Modulator and FIR Filter Outputs

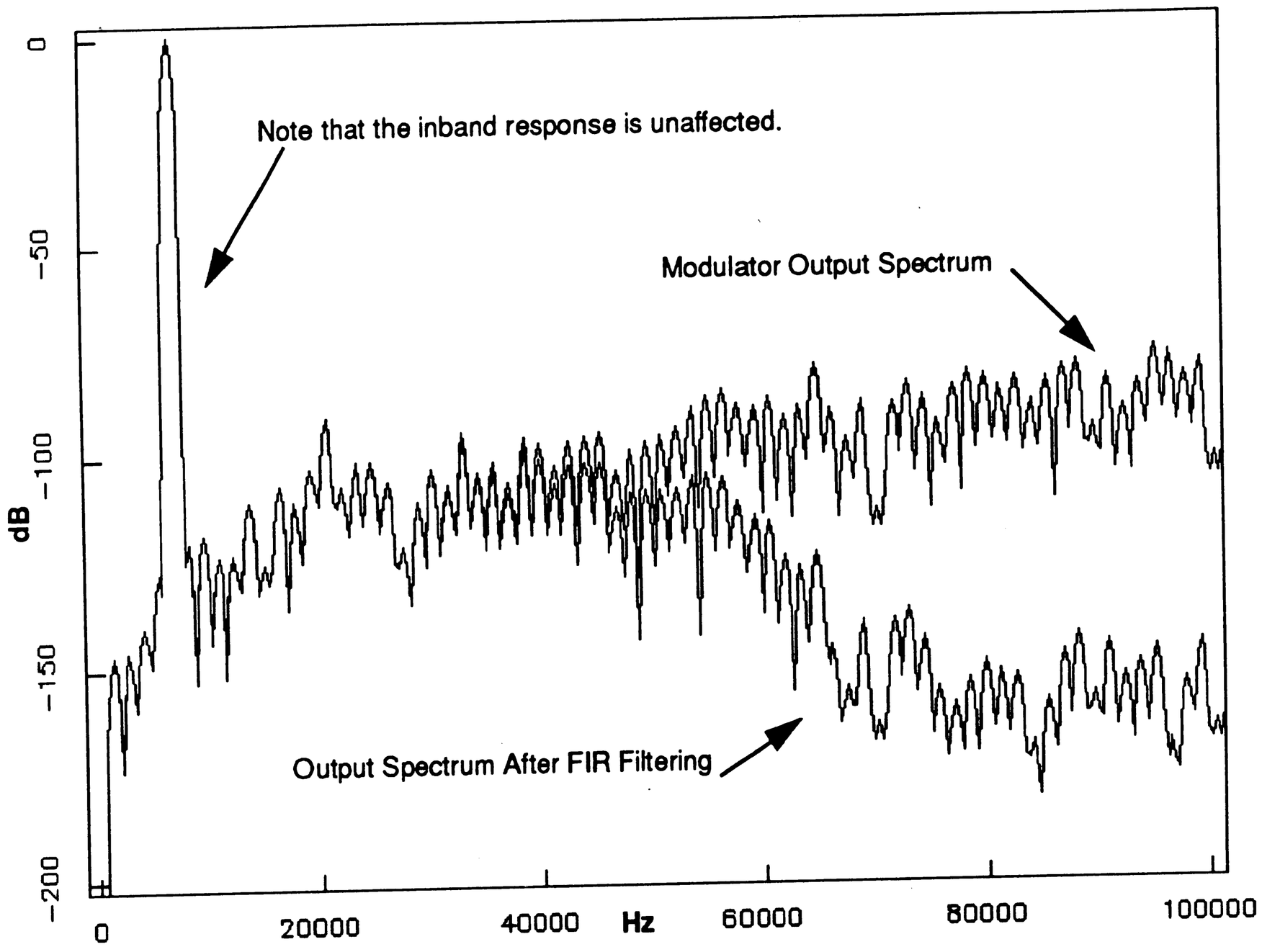
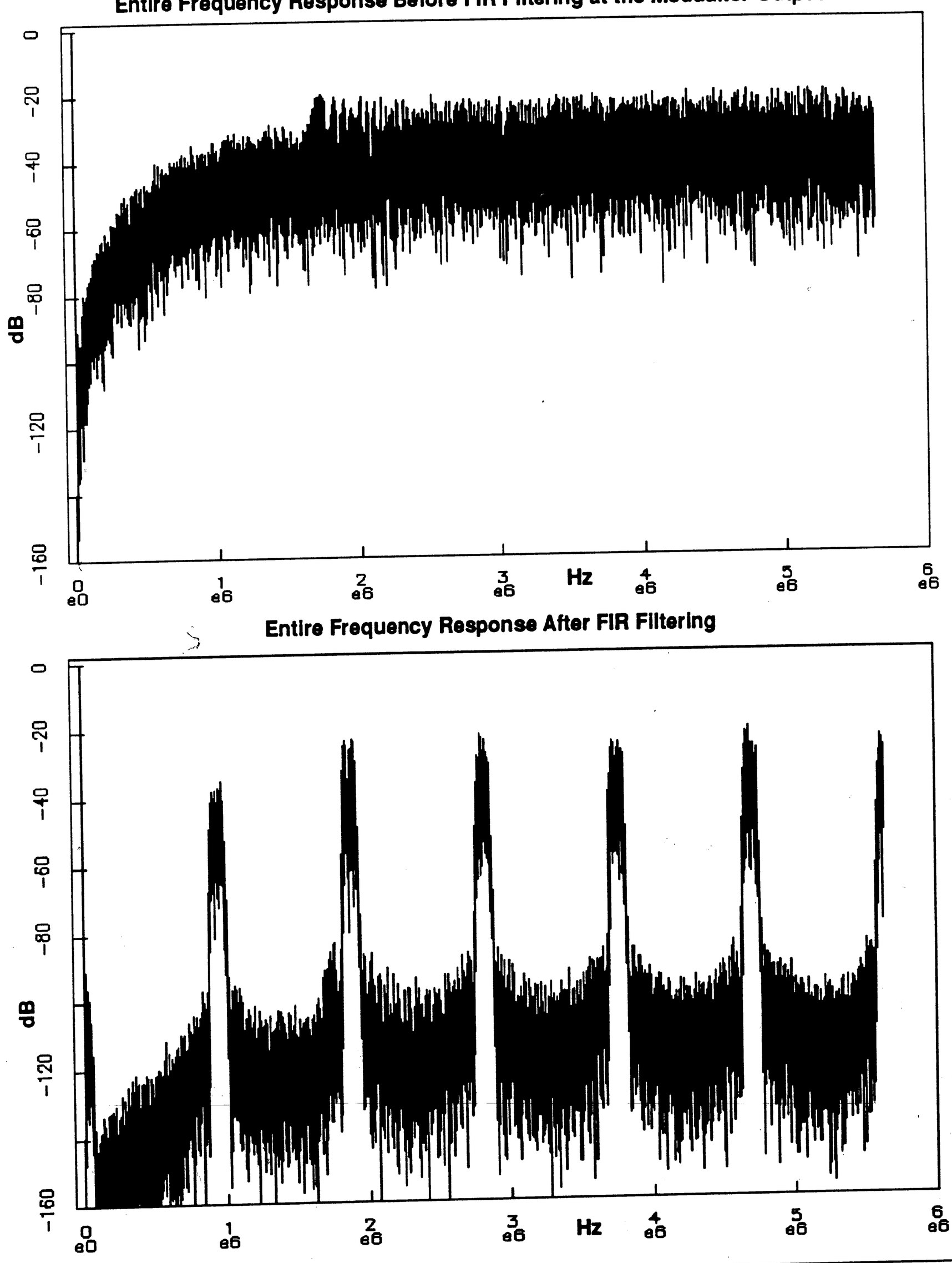


FIGURE 27 shows the entire spectrum for the modulator before and after FIR filtering. The FIR filter has removed the high frequency quantization noise energy from the modulator output except where the repeated passbands occur due to decimation. As predicted, the FIR filter has provided a quick cutoff at the passband edge giving the analog post-filter time to become effective while not impacting upon the baseband response.

FIGURE 27 Entire Frequency Spectrum of the DAC Output



3.2 The Switched-Capacitor DAC

The next area that needs attention is the convolution or summation process, which converts the digital signal back into the analog domain.

3.2.1 What Type of DAC, a Simple DAC or an Integrating DAC

Because the system operates at 11.28 MHz, the conversion period is 90ns. In a SC implementation, a 2-phase clock is required. In many simple SC DACs, the output capacitor is zeroed out during one of these phases. This requires that the op amp be fast enough to handle transients from this zero level to full scale output in one half of a conversion period. This implies that the op amp would be required to slew and settle a 100pF load approximately 1 Volt in 44nS. This would require a bias current of 23mA (113mW) just in the input stage of the op amp.

Since the digital audio input signal is band-limited to 20kHz, it would be advantageous to use a circuit that does not require such fast slewing. By using a DAC that holds the previous output value instead of zeroing, the maximum slew rate is reduced to that of a full scale 20kHz output. For example if a full scale 20Hkz sine wave is the input signal, then at its center where the slew rate is the fastest, the DAC output should only change by 0.61% (1 part in 163) of the reference level. This also has the advantage of introducing a pole in the output response, helping to filter the output signal. Since an output change of at most only a fraction of the reference voltage is ever needed, a lower power level can be used in the summing amplifier.

3.2.2 How Accurate Must the Symmetry Introduced Third (Zero) Level Be?

By taking advantage of the coefficient symmetry, the filter length can be cut in half. This requires that the DAC also generate an intermediate zero level in addition to the +/- reference levels which raises the question of what will distortion be generated if the zero level is not in the exact center of the reference range. Because errors in the coefficient values do not produce harmonic distortion but slightly lower stopband attenuation, however the zero offset should not produce additional distortion.

By computer simulation this can be verified by observing the FIR filter's frequency response and distortion performance using a zero-level mismatch. In the time domain, no distortion was noticed even with a 1% zero mismatch. In the frequency domain, FIGURE 28 shows the effect of the mismatch on the FIR filters frequency response and stopband attenuation. The baseband spectrum as shown in FIGURE 29 remains unchanged by the mismatch.

FIGURE 28 Effects of Zero Level Mismatch in the FIR Filter Response

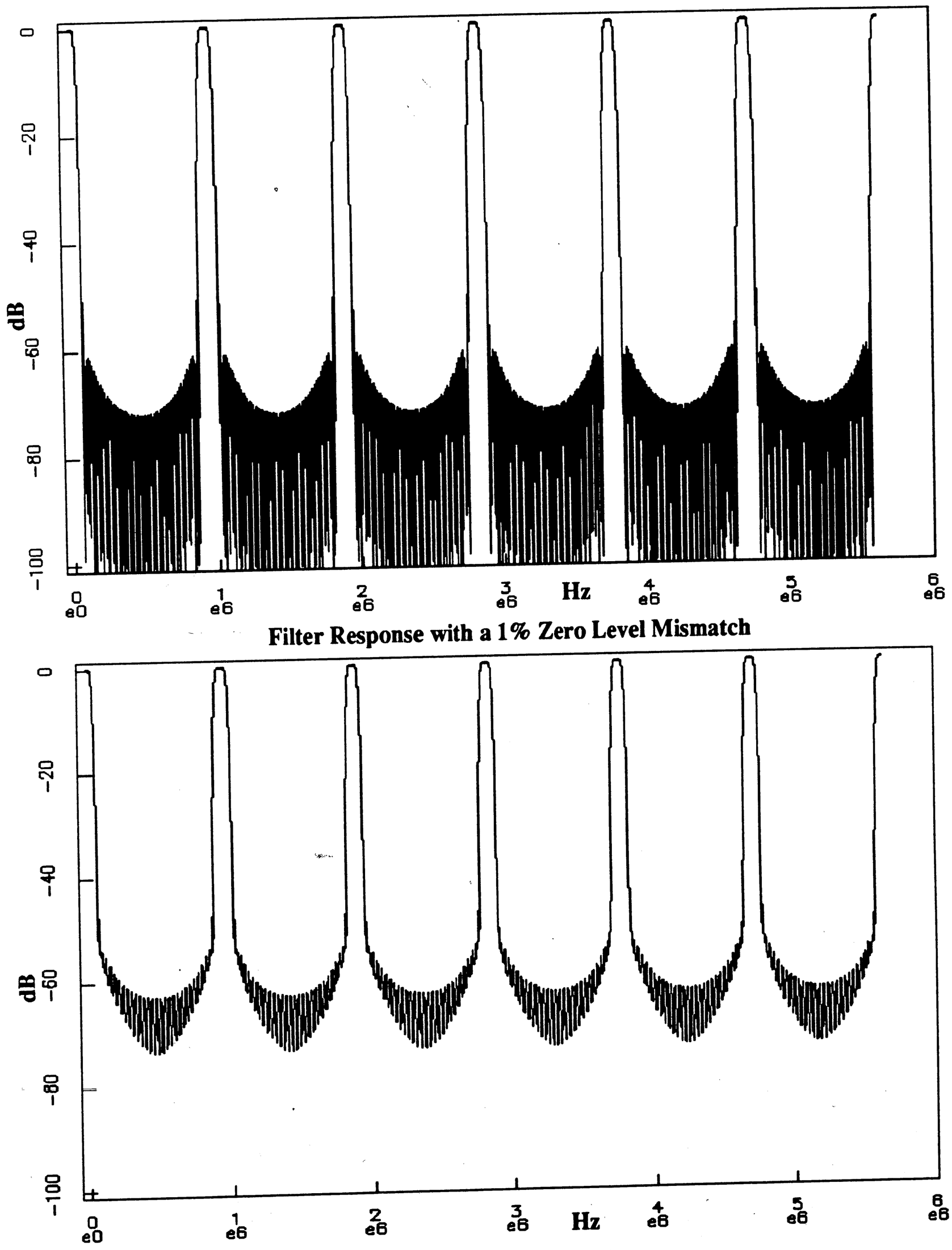
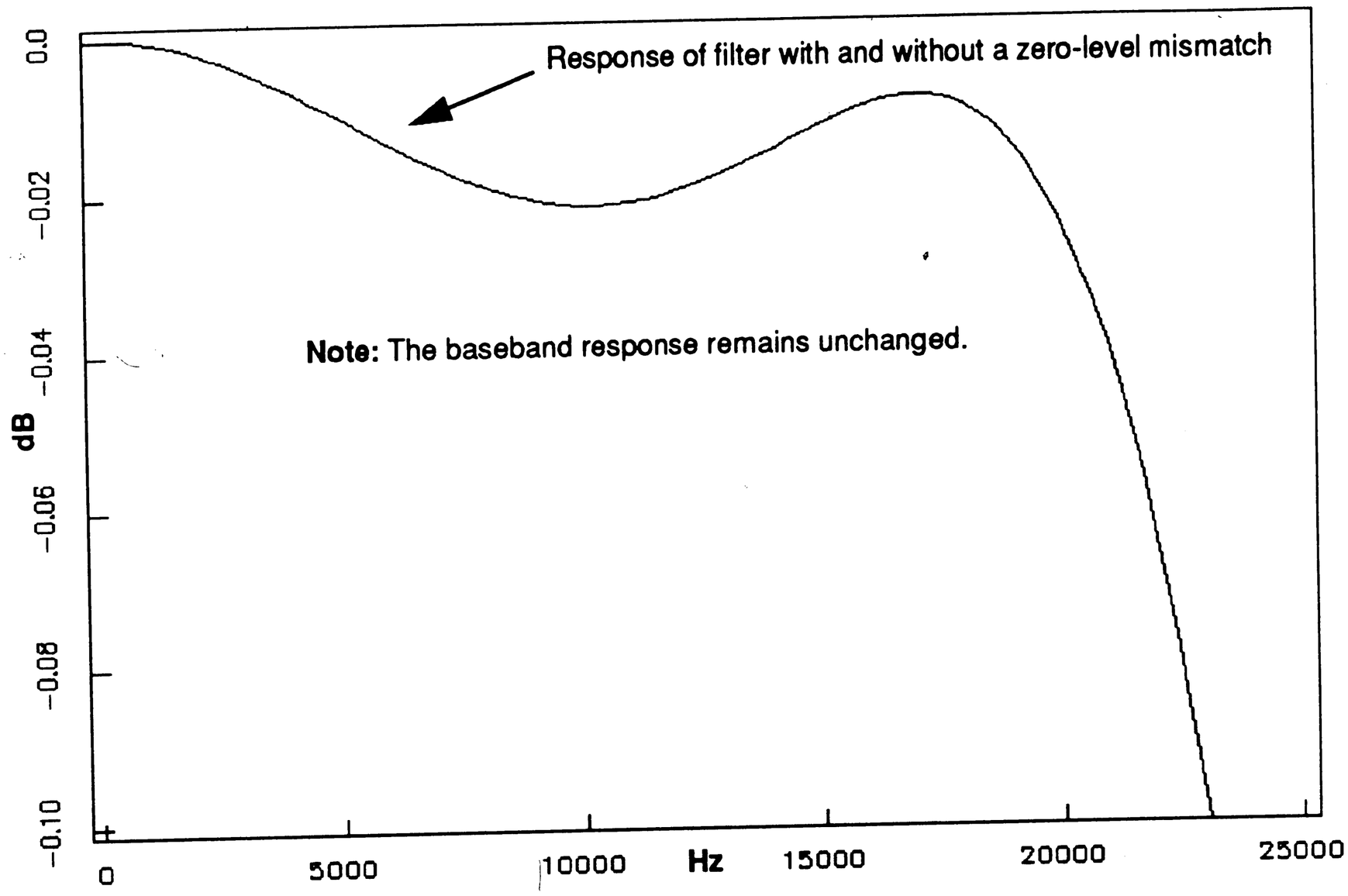


FIGURE 29 Baseband Response of the FIR Filter with a Zero-Level Mismatch



3.2.3 What Opamp Speed, Gain and Noise Performance is Required

Since the digital audio input signal is of 16-bit precision, the DAC system must meet that performance level thereby setting the requirements on the opamp. As discussed in section 3.2.1 on page 42, the opamp must settle to 16-bit precision in 44ns but it does not need a large slew rate if an integrating architecture is used.

The op amp open-loop gain requirements are modest since this gain primarily affects the conversion gain. A small error in the conversion gain can easily be ignored or compensated for in other ways. More important is the ability of the op amp to handle the large dynamic range of digital audio. The open-loop gain only needs to be sufficient to keep the closed-loop distortion below the 16-bit level. If the summation opamp is of the integrating type, with a single pole response then only the opamp noise in the frequency range of 0 to 20kHz needs to be considered. With a full scale output of 1 Volt, a closed-

loop gain of 1, a 20kHz bandwidth and the desire to keep the noise level 100dB below full scale the input referred opamp noise must be below 70 nV/$\sqrt{Hz}$.

4.0 Conclusions and Future Work

Presented in this thesis has been a method for performing digital audio quality D/A conversion with reduced cost and complexity without compromising performance. The thesis first presents a short introduction to digital audio and then proceeds to present background information on D/A conversion techniques, Sigma-Delta modulation, FIR filtering and Switched-Capacitor DACs. These various elements will comprise the new digital audio DAC architecture introduced in this thesis. Also reviewed were several state of the art digital audio DACs emphasizing advantages, disadvantages and unique points of each design. Next the combination of a switched-capacitor DAC and a FIR lowpass filter was introduced as the main topic for this thesis. Finally an actual block level and functional circuit design was presented.

Using the DAC architecture presented in this thesis, a digital audio quality DAC is achievable that gives improved frequency response performance. This converter would be more economical to manufacture since it does not require the precision matching of elements as typically required by other digital audio converters.

4.1 The FIR Lowpass Switched-Capacitor DAC

It was shown that to achieve the desired system performance, the FIR filter length would be on the order of 1000 taps. Since this many taps is impractical from a SC- DAC standpoint, impulse response decimation, linear-phase coefficient symmetry and an analysis of the design trade-offs was necessitated. With these techniques, the number of needed coeficients for the combined DAC and FIR filter was reduced from 817 to 32. By using the linear phase impulse response coefficient symmetry, a third DAC level was introduced without a strict requirement on its linearity.

4.1.1 How have the Analog Post-Filtering Requirements Been Affected

The analog post-filtering requirements have become easier to meet by using this FIR filtering technique when compared to more conventional oversampled digital audio DACs. As stated earlier the FIR filter provides a passband response (0 to 20kHz) linear within 0.02dB yet has its response down by

60dB at 80 kHz without affecting the passband phase response. To do that with an analog filter, at least a 5th order filter is required. To achieve this quick cutoff would require a FIR filter length of 745 taps, although by decimating the impulse response, the number of active taps in the convolution can be reduced. For this thesis a decimation factor of 12 was chosen reducing the number of active tap to 32.

Decimating the impulse response causes the frequency response of the filter to become repetitive such as in a comb filter. For the FIR filter designed here, the first repeated passband occurs at 940kHz. It is this repeated passband that sets the requirements for the analog post filter since it must provide the attenuation for the repeated passbands. It was determined that with 3 poles at 200kHz the DAC output spectrum becomes acceptable and the poles are far enough from the passband so that they do not affect the passband phase response.

4.2 For the Future

This thesis has laid out the ground work for a novel digital audio quality D/A conversion architecture and has suggested requirements for the FIR filter DAC portion of this architecture. Remaining to be designed are the design of a Sigma-Delta modulator, interpolator and pre-filter to translate the 16-bit digital audio data into the one-bit stream needed to drive the combined filter and D/A. Eventually a complete design in silicon must be done and evaluated.

Due to the large number of interrelated variables controlling the system performance, searching the design space for the optimum combination can be quite time consuming and expensive. For this thesis, being limited on both time and expense, only a quick attempt was made to find an acceptable combination. Therefore when more time is available, more searching of this design space would be advisable.

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6.0 VITA

H. Scott Fetterman was born December 15, 1958 in Coaldale, Pennsylvania. He is the son of Harry C. Fetterman and Norma D. Fetterman of Tamaqua, Pennsylvania. He attended Tamaqua High School graduating in 1976, and then attended the following other institutions:

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The Pennsylvania State University	Bachelor of Science in Electrical Engineering Technology	1983
Lehigh University	Anticipating Masters of Science in Electrical Engineering	

Currently Mr. Fetterman is employed at AT&T Bell Laboratories where he is involved in the design of analog MOS integrated circuits for the telecommunications field. He has co-authored one paper entitled "A 14-bit 80-kHz Sigma-Delta A/D Converter: Modeling, Design, and Performance Evaluation," with Steven R. Norsworthy and Irving G. Post published in the *IEEE Journal of Solid-State Circuits Vol. 24 April 1989 pp.256-266.*